

Press Release

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FOR IMMEDIATE RELEASE

NeuroMatrix[®] Architecture Is Chosen as a Part of the Best DSP Third-Party Program in the Industry

MOSCOW, Russia January 28, 1999 - MODULE Research Center, the owner of NeuroMatrix[®] DSP architecture (patent pending) joins Texas Instruments "Customer Choice Third-Party Network" (www.ti-dsp.com). The TI's Third-Party Program is designed to assist about 170 TMS320 third parties worldwide in gaining exposure for their products and service and helping them align with TI business strategies. RC "Module" has been established in 1990 by well known Russian firms of military-industrial complex - Interstate corporation "Vympel" and its research institute for radio devices (RIRD), entered to the program with its new product - NM6403 processor. RC "Module" is a rapidly progressing company known among the leading Russian and overpasses' companies engaged in the design and development of embedded computer systems based on modern electronic components and technologies. RC "Module" has a staff of highly qualified engineers and scientists using the most modern design tools such as Cadence and Synopsys and prototype manufacturing equipment, which permits a very short design cycle (few months) from the concept or idea to the finished prototype ready for mass production.

Although RC "Module" was founded nine years ago, the microprocessor division was established in 1995. The first goal of the division was designing the architecture and chip for best support of original neural network and image processing algorithms developed by RC "Module". Due to the usage of TI TMS320C40 DSP for accelerating boards since 1994, there was a lot of application software designed and optimized for TI's DSP architecture. That was one of important things to design the processor with communication capability to TI 'C40 DSP. The NeuroMatrix[®] processor architecture was developed in 1996. It includes 32-bit RISC core, 64-bit VECTOR core and two communication ports hardware compatible with TI TMS320C4x. The NM6403 DSP is a first hardware implementation of the architecture produced using SAMSUNG 0.5-um CMOS technology appeared in 1998. The main feature of NM6403 processor is a programmable operand width and scaleable performance from 50 MMAC (32-bit data) up to 51.2 GMAC (1-bit data) at 50 MHz clock rate. The communication ports allow to use NM6403 as a vector-matrix co-processor for multiprocessor systems based on TI 'C4x DSP. The processor is able to perform a broad range of DSP applications. Thus, the 256-point 32-bit complex Fast-Fourier Transform (FFT) performs in 4070 clock cycles and require only 80 microseconds, the Walsh-Hadamard Transform (WHT) with 2M points calculates for 0.34 seconds, the Forward Propagation (1024 layers, 1024 neurons/layer) neural network emulates for 1.53 seconds, "Sobel" 2D filter performs 37.5 frame (384x288 pixels)/second.

NM1 Dual-CPU is a first PCI board based on NM6403 DSP. The board contains two NM6403 processors, up to 8 Mbytes static memory, 64 Mbytes dynamic memory. The performance of NM1 for vector-matrix calculations is 1.9 billion operations per second. The board has four communication links which allow easy connection to any Third-Party DSP boards based on TI 'C4x. The development tools for PC host platform includes an ANSI X3J16/95-0029 preliminary standard compatible C++ compiler, an assembler, an instruction level simulator, a cycle accurate simulator, a linker, a source level debugger, a load/exchange library and set of application specific vector-matrix libraries. The vector-matrix optimized library simplifies C-language programming and allow to design the DSP and telecommunication applications. The NM6403 Verilog silicon proven model and test bench is also provided for system level simulation and PCB design.

The Single-CPU one-size TIM (Texas Instruments Module) based on NM6403 DSP will be available on July 1999.

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