

EDN's 2003 DSP directory

DSP shipments were tracking at 5% growth for 2002 until shipments in December ballooned. According to market-research company Forward Concepts (www.forwardconcepts.com), this balloon in shipments netted an overall DSP-revenue growth of 14.1% for 2002. Wireless applications, commanding 65.8% of DSP dollars in 2002, remain the market movers for DSP shipments this year. Forward Concepts predicts that semiconductor-market growth this year will not be “above normal” and forecasts a 20% growth for the DSP market for 2003.

Despite some vendors withdrawing from the DSP market over the last year, this year’s directory contains more entries than ever before. StarCore began its existence as a stand-alone company late 2002. The directory no longer lists some products from the member companies of the technology center such as Agere’s StarPro2000. Also, the design team for the Carmel DSP core is now part of StarCore, and the Carmel core is no longer available for licensing. Another DSP-core-design-team move means you can find last year’s DSP Group family of cores in the directory under ParthusCeva.

To maintain a clear distinction between DSP and controller devices, the directory survey requested devices, cores, or extensions that not only can process signals, but also find primary use in signal processing. The DSPs have to be software-programmable devices, cores, or extensions that include an assembler or a compiler in the tool set. This stipulation eliminates products that, although they may include a programmable DSP core, restrict users to only selecting and setting operating parameters. Also, listed devices or intellectual property must be currently or soon available. Even with these criteria the directory still grew.

The directory lists entries alphabetically by vendor and consolidates the development-support section in the last entry for each vendor’s section. This structure reduces the amount of duplicate information, and more important, it emphasizes that tool sets are usually common across a vendor’s product lines. Also, without exception, integrated tool sets are a strategic element of any DSP offering and play a large role in design wins. The directory index groups entries by processor size rather than directory location to facilitate the comparison of similar-sized processors.

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ADELANTE TECHNOLOGIES SATURN

at a glance:

- The core area measures 0.5 mm² and consumes 0.25 mW/MHz in a standard 0.18-micron CMOS process.
- The Saturn can perform 420 MMACs (million MACs)/sec at 210 MHz.

Adelante’s Saturn is an extensible, low-power, small-area, “open” DSP core and subsystem targeting wireless-baseband handsets and digital-control applications. It employs a dual Harvard architecture with two 16-bit multipliers, four 16-bit ALUs that can combine into two 40-bit ALUs (32 bits with 8 bits of

overflow), a shift-and-saturation unit, a bit-manipulation unit, a barrel shifter, a hardware-loop-control unit, a program-control unit, and two data memories that are configurable to 64k words and expandable to 1M word with paging. The designer extends the core via custom application-specific instructions, execution units, and coprocessors to accelerate repetitive tasks.

The Saturn core integrates into Adelante's Lunar DSP subsystem, which includes program and data memory, DMA, interfaces to external processors, peripherals, and I/O (including an AMBA bus for ARM and MIPS processors); BIST; and JTAG hardware-debugging capability. Special constructs in the three-stage pipeline enable single-cycle-overhead short branching and zero-overhead long branching. One nonmaskable and 16 maskable interrupts with single-cycle interrupt switching and simultaneous shadow X/Y-address pointer switching support immediate execution of service routines.

Addressing modes: The Saturn supports single- and dual- data-memory-operand addressing for 32-bit operands, with direct data and absolute addressing. Offset, indirect, absolute, immediate, modulo, and bit-reversed addressing support bit/nibble/byte access to memory. Two of the three X/Y-address pointers are context-sensitive.

Special instructions or integral-peripheral functions Designers can extend the Saturn's 16-bit instruction set with 256 application-specific 96-bit VLIW (very-long-instruction-word) instructions that can fully exploit all core resources in parallel to accelerate repetitive DSP functions (for example, two-cycle execution of a 12-operation Viterbi butterfly). Designers can also integrate application-specific execution units and coprocessors into the DSP subsystem to accelerate computationally intensive functions, such as turbo coding or multichannel ADPCM (adaptive differential pulse-code modulation).

Development support: The Atmosphere development environment supports code-development debugging for application-specific instructions and execution units. The code-development tools include a compiler, a linker, a debugger, an instruction-set simulator, and a profiler. The debugger supports use with a JTAG hardware debugger and the runtime-debugging block for in-circuit runtime emulation. Adelante offers design services for the development, integration, and verification of application-specific execution units and application-specific coprocessors.

AGERE SYSTEMS DSP16XXX

at a glance:

- The DSP16410 can perform 800 MMACs (million MACs)/sec at 200 MHz.

Agere's DSP16210 and DSP16410 devices use the DSP16000 core and target digital-communications applications that benefit from large, on-chip RAM with downloadable system support. The DSP16210 includes 60k words of dual-port RAM and can address as many as 192k words of external storage in both its code/coefficient-memory address space and data-memory address space. An internal boot ROM includes system-boot code and hardware-development system code. This device also contains a bit-manipulation unit; a two-input, 40-bit ALU with add/compare/select for enhanced signal-coding efficiency and Viterbi acceleration; and a three-input adder for single-cycle accumulation of the results of both multipliers. To optimize I/O throughput and reduce the I/O service-routine burden on the DSP core, two modular I/O units manage the simple serial-I/O port and the 16-bit parallel host-interface peripherals. They also provide transparent DMA transfers between the peripherals and on-chip,

dual-port RAM.

The DSP16410 targets communications-infrastructure applications and features twin DSP16000 dual-MAC (multiply-accumulate) DSP cores and enhanced DMA capabilities. Each DSP core has access to a 192-kbyte block of memory (384 kbytes total) and share a 4-kbyte block of memory for interprocessor communications. The DSP16410's large on-chip memory supports fixed-point signal-processing functions, including equalization, channel coding, compression, and speech coding. A centralized DMA unit supports transparent peripheral-to-memory and memory-to-memory transfers. The DSP16410 includes a 16-bit parallel port with DMA support that can provide host access to all DSP memory. The two serial-I/O units also include DMA support, are compatible with TDM highways, and include hardware support for u- and A-law companding.

Addressing modes: The DSP16000 core architecture supports immediate, register-direct, address-register-indirect, and program-counter-relative modes, as well as register-plus-displacement addressing, and circular-buffer addressing.

Special instructions or integral-peripheral functions: The special instructions are arithmetic, logical, and shift operation, and bit-manipulation instructions to implement nonlinear algorithms, such as signum, A- and u-law conversions, half- and full-wave rectification, and rounding. The bit-manipulation instructions include barrel shifting, normalization and exponent computation, and bit-field insertion or extraction.

Development support: Agere's LUxWorks supports development for DSP16000 devices. The integrated system-level development tools include a C compiler, an assembler, a linker, and a simulator. Hardware-development platforms and in-circuit-emulation capabilities are available through Agere's TargetView JTAG communication system, featuring Agere's DART (Data Access in Real Time) for real-time data collection. Agere also provides optimized libraries for voice transcoding and echo cancellation for wired networks and 2, 2.5, and 3G wireless standards.

ANALOG DEVICES ADSP-21XX

at a glance:

- All ADSP-21xx processors are source-code-compatible.
- Devices cost less than \$4 in high volume.

All ADSP-21xx processors are source-code-compatible and feature a high-level algebraic programming syntax. All instructions, including multifunction instructions, execute in a single clock cycle. ADSP-21xx processors use separate program and data buses operating on 24-bit instructions and 16-bit data. The wider instruction word allows the device to use a more complex and robust instruction set than a 16-bit operation code, and the 16-bit data word provides lower power consumption for the necessary dynamic range. These processors include as much as 2.4 Mbits of on-chip SRAM and integrate a programmable DMA controller to maximize I/O throughput. The ADSP-218x supports as much as 4 Mbytes of external memory, and the ADSP-219x architecture supports 16M words of external memory. All processors support a variety of serial-communications interfaces to ADCs, DACs and other processors.

Addressing modes: ADSP-21xx processors support immediate, register-direct, memory-direct, and register-indirect addressing modes. The ADSP-219x adds register, indirect-post-modify, immediate-modify, and direct- and indirect-offset addressing modes. Each address generator supports as many as four circular buffers, each with three registers. The ADSP-219x supports as many as 16 circular buffers using a data-address-generator shadow-register set and a set of base registers for additional circular-buffering flexibility.

Special instructions or integral-peripheral functions:The ADSP-21xx contains dedicated loop hardware and a “do-until” loop instruction that supports loops ranging from 0 to 16,000 iterations, or loops, with infinite iterations. The ADSP-218x supports four-deep nesting via its loop hardware, and the ADSP-219x supports as many as eight loops. In addition to the standard arithmetic and logic instructions, the ALU supports division primitives. The ADSP-219x program-sequencer features a six-deep pipeline and supports delayed branching. The ADSP-219x buses and instruction cache provide the data flow to maintain a continuous execution rate.

ANALOG DEVICES ADSP-21XXX SHARC

at a glance:

- Devices natively support 32-bit fixed, 32-bit IEEE floating, and extended 40-bit floating-point data types.
- Multiprocessing configurations require no glue hardware.

The ADSP-21161N is the latest member of the SHARC family of general-purpose programmable DSPs. It uses a Super Harvard Architecture and has both SIMD (single-instruction-multiple-data) and SISD (single-instruction-single-data) functions. Each of the two computational blocks in the SHARC SIMD core includes a multiplier, an ALU, a data-register file, and a barrel shifter that can process in parallel in SIMD mode. The core contains dual data-address generators, independent data- and address-memory buses, a program sequencer with zero-overhead looping, an instruction cache, and a timer. While the core operates at full speed, the I/O processor moves data on and off chip. SHARC DSPs integrate 1 Mbit to 4 Mbits of on-chip SRAM; as many as four serial ports, six link ports, and 14 zero-overhead DMA channels; an SPI-compatible port; a synchronous-DRAM controller; a parallel host interface; cluster multiprocessing support; and an IEEE JTAG standard 1149.1 test-access port with on-chip emulation. The two independent, on-chip, dual-ported SRAM blocks are selectable between program and data memory. The independent synchronous serial ports operate in TDM multichannel mode and, on the ADSP-21065L and ADSP-21161, offer $\mathcal{F}S$ mode, which is useful for audio applications.

Addressing modes: ADSP-21000 SHARC DSPs support absolute and relative-direct addressing, premodify and postmodify registering, immediate-value-indirect addressing, and modulo and bit-reversal addressing. The dual-ported memory allows independent data transfers from the core and the I/O. Three on-chip buses allow two data transfers from the core and one from I/O in one cycle.

Special instructions or integrated-peripheral functions:The ADSP-21000 SHARC family features distributed on-chip bus arbitration. These devices allow you to connect as many as six processors (two for the ADSP-21065L) in parallel, plus a host. All SHARC instructions execute in one cycle. Special

instructions include bit manipulation, division iteration, reciprocal of square-root seed, conditional subroutine call, single and block repeat with zero-overhead looping, average of two numbers, bit packing and unpacking fixed to and from floating-point conversion, and conditional execution of most instructions. SHARC supports IEEE-754 single-precision floating-point, 32-bit fixed-point, and a 40-bit extended IEEE format for additional accuracy.

ANALOG DEVICES ADSP-215XX BLACKFIN

at a glance:

- System architecture supports an integrated DSP and RISC microcontroller-unit instruction set.
- Dynamic power management minimizes power consumption for power-constrained applications.

Blackfin DSPs feature dual-MACs (multiply-accumulate) units, 300-MHz clock rates, and dynamic power management for balancing system performance and power consumption. The modified Harvard architecture core combines signal- and control-processing features into a single instruction-set architecture that benefits programming in high-level languages, such as C/C++. DSP-core functional blocks and capabilities include two 16-bit MAC units, two 40-bit ALUs, four 8-bit video ALUs, and a barrel shifter, plus eight 32-bit math registers with support for 8/16/32-bit integer and 16/32-bit fractional data types. The four 8-bit video ALUs address multimedia algorithms including MPEG-2, MPEG-4, and JPEG, allowing one device to concurrently process audio, video, imaging, and data information. The ADSP-21535 targets next-generation digital-communication systems and Internet appliances, and the ADSP-21532 targets consumer multimedia systems.

Blackfin DSPs support user and supervisor modes, byte addressing, memory protection, and an orthogonal RISC instruction set. All Blackfin DSPs support a hierarchical and configurable memory model. L1 memory is physically closest to the core for highest system performance and is configurable as either SRAM or cache. L2 memory provides a larger memory space suitable for bulk storage of instructions or data. Additionally, dynamic power management permits context-sensitive control over power consumption by enabling designers to dynamically vary both the operating frequency and voltage of the DSP core for optimizing power-consumption profiles.

Addressing modes: All Blackfin devices support DSP and general-purpose addressing modes, including indirect, indexed, autoincrement or autodecrement, postautoincrement, and bit-reversed. Four sets of index, base, length, and modify registers enable circular (modulo) buffering of as many as four buffers per data-address generator. In addition, eight 32-bit registers are available for general-purpose addressing of 8-, 16-, and 32-bit data.

Special instructions or integral-peripheral functions: The Blackfin instruction set includes special instructions for video and next-generation communications algorithms. Video-pixel-manipulation instructions include quad-byte operations for sum-absolute difference, average, and pack/unpack. Communications algorithms use dual-MAC instructions with rounding and saturate options in addition to add/compare/select or vector operators.

ANALOG DEVICES ADSP-2199X

at a glance:

- Processors target mixed-signal, embedded-control, and signal-processing applications.
- Devices integrate a 160-MIPS DSP with a 14-bit, 20M-sample/sec ADC.

The ADSP-2199x family encompasses high-performance, mixed-signal DSPs that maintain full code compatibility with ADSP-219x processors. These devices integrate mixed-signal components, such as high-resolution ADCs, with a variety of peripheral components to form single-chip devices targeting embedded-signal-processing and -control applications, such as industrial measurement and control, high-end servo-motor drives, uninterruptible power supplies, high-end switched-mode power supplies, optical-networking control, and intelligent-sensor interfaces.

The ADSP-21990, ADSP-21991, and ADSP-21992 integrate a 16-bit ADSP-219x core, operating as fast as 160 MHz, with a 4k- to 32k-word program memory; a 4k- to 16k-word data memory; and an eight-channel, 14-bit, 20M-sample/sec ADC core, with dual S/H amplifiers for simultaneous sampling. An external memory interface enables direct access to as much as 1M word of external memory for program-memory expansion, data-memory expansion, or both. ADSP-2199x devices are available in industrial- and automotive-temperature (ADSP-21992 only) ranges and packaged in both MBGA and LQFP versions.

Addressing modes: Identical to the ADSP-219x products, the ADSP-2199x products support immediate, register-direct, memory-direct, register-indirect, indirect-postmodify, immediate-modify, an direct- and indirect-offset addressing modes. The ADSP-2199x supports as many as 16 circular buffers using a data-address-generator shadow register and a set of base registers for additional circular-buffering flexibility.

Special instructions or integral-peripheral functions: ADSP-2199x devices share all of the architectural features and special instructions of the ADSP-219x core. The key integrated peripheral of these products is the high-performance, 14-bit ADC. The embedded-control peripherals include a three-phase PWM generation unit; a 32-bit incremental-encoder interface; dual auxiliary PWM outputs a watchdog timer; and general-purpose peripherals, such as timers, digital I/O lines, and serial-communications and programmable-interrupt controllers. Additionally, these devices include an on-chip precision-voltage reference and an integrated power-on-reset circuit.

ANALOG DEVICES ADSP-TS101 TIGERSHARC

at a glance:

- TigerSHARC can perform 1500 Mflops or 2000 16-bit MMACs (million MACs)/sec at 250 MHz.
- The device targets wireless-infrastructure and multiprocessing applications.

The ADSP-TS101S TigerSHARC DSP is a floating-point DSP targeting multiprocessing and 3G wireless-infrastructure applications. This static superscalar architecture blends the best features of DSP, RISC, and VLIW (very-long-instruction word) for a high-performance DSP architecture. These features

include a load/store architecture, branch prediction, a large interlocked register file, fast mathematical computations, bit reversing, zero-overhead looping, background data movement with DMA, and an instruction width that varies from one to four words. Two computational blocks in TigerSHARC devices support 1-, 8-, 16-, and 32-bit operations. Each computational block contains a 32-entry register file, an ALU, a multiplier, and a shifter. It can execute two 32-bit floating-point MACs (multiply accumulates), eight 16-bit MACs with 40-bit accumulation, or two 16-bit complex MACs in one cycle. The device can perform as many as 32 mathematical operations per cycle with 8-bit data types. Three 128-bit buses support TigerSHARC's three on-chip memory banks, which total 6 Mbits. In a given cycle, the processor can fetch four 32-bit instruction words and load 256 bits of data into the register file or store it in memory.

Addressing modes: TigerSHARC has two integer ALUs in addition to the two computational blocks. It uses the ALUs primarily for data-address generation, and each unit contains a 32-bit ALU and a fully orthogonal 32-word register file. These units can generate an address per cycle that allows the device to send two 128-bit words to each computational unit. These units also support preaddress and postaddress modification, circular buffering, and bit reversing without an extra-cycle penalty.

Special instructions or integral-peripheral functions Special instructions to accelerate both symbol- and chip-rate processing for 3G baseband-signal processing, include a complex MAC operation for chip-rate processing and add/compare/select operation for channel-decoding algorithms. Peripherals include four bidirectional link ports, a 14-channel DMA controller, and a 64-bit-wide external port that includes an SDRAM controller, a host interface, and support for glueless multiprocessing of as many as eight TigerSHARCs. The four link ports are byte-wide interfaces that transmit data on both the rising and the falling clock edge and offer a second method for multiprocessing with ring and 2-D mesh multiprocessing configurations.

Development support: The CrossCore development components include the VisualDSP++ software-development environment, EZ-Kit Lite evaluation systems, emulators, and DSP/math libraries. VisualDSP++ is an integrated software-development environment that includes an assembler, a C/C++ compiler, a linker, a debugger, an archiver, a loader utility for creating bootable images, VDK (VisualDSP++ kernel), advanced plotting tools, and statistical profiling. The EZ-Kit Lite evaluation system supports extension by the addition of JTAG in-circuit emulation. Emulators are available for serial-port, PCI, and USB host platforms. The VisualFone is the development system for SoftFone-based products. A complete GSM/GPRS protocol stack for SoftFone is available from TTCCom.

ARC ARCTANGENT

at a glance:

- Cores support a user-customizable instruction set, registers, buses, interrupts, caches and memories.
- You can integrate preverified peripherals, such as, USB 1.1 and 2.0, Ethernet media-access controller, and UART, using the ARChitect.

The ARCTangent-A4 and ARCTangent-A5 cores are synthesizable, user-customizable, 32-bit RISC processors with optional DSP extensions. Developers can add extension instructions, configure caches,

integrate peripherals, and add DSP extensions with the ARChitect configuration tool, a graphical-design tool that generates RTL files and synthesis scripts. The ARctangent-A4 uses a 32-bit instruction set, and the ARctangent-A5 uses the ARCompact 16/32-bit instruction set that allows free mixing of 16- and 32-bit instructions for greater code density without mode-switching penalties. Both cores are synthesizable with industry-standard tools and are portable to almost any foundry or process. The integrated RISC/DSP cores allow programmers to use a single tool chain for RISC and DSP software development.

Addressing and processing modes: The ARctangent supports as many as four banks of XY memories from 512 bytes to 16 kbytes and has a user-extendable register file. The address-generation units for the XY memories support modulo and bit-reverse addressing with variable-offset preincrement and postincrement modes.

Special instructions or integral-peripheral functions DSP features include 16×16-, 24×24-, and dual 16×16-bit MAC (multiply-accumulate) operations with 8 guard bits for the accumulator, saturating addition and subtraction instructions, fractional arithmetic, normalize (find first bit), swap, minimum/maximum, 32×32-bit barrel shifter, 32×32-bit multiplier, and zero-overhead loops. The instruction set is conditional, with as many as 16 user-defined condition codes. Developers can also configure and extend the instruction set to optimize performance for specific applications.

Development support: The ARctangent RISC/DSP comes with RTL source code, extensive documentation, the ARChitect tool, MetaWare C/C++ Compiler and SeeCode debugger, an assembly-language DSP-function library that is callable from C/C++ programs, customer training, and technical support. The single tool chain supports both RISC and DSP software development. ARC also provides preverified and integrated peripheral intellectual-property cores, including USB, Ethernet, and driver software; the Precise/MQX RTOS; network-protocol stacks; and software for vertical-market consumer and communication applications. Third-party support includes emulator support from Corelis (www.corelis.com) and Ashling Microsystems (www.ashling.com) with memory-system support from Denali (www.denali.com).

BOPS MANARRAY

at a glance:

- The core has power consumption of 11 to 36 mW for as many as 4000 MIPS.
- BOPS Halo Compiler achieves an EEMBC (*EDN* Embedded Microprocessor Benchmark Consortium) Telecom Benchmark score of 181.

The ManArray fully scalable, configurable, synthesizable DSP architecture is programmable and reusable in an array of implementations for communications, mobile-multimedia, and wireless applications. Each application-specific family balances the trade-offs in cost, power, and performance for targeted applications. The MoCARay configuration targets GPRS/EDGE (general-packet-radio-service/enhanced-data-rate-for-GSM-evolution) baseband layer 1 processing at less than 20 mW and turbo-codec processing at less than 50 mW for software-defined trimode 2, 2.5, and 3G handsets. The MICoRay configuration targets full-duplex MPEG-4 CIF codec processing at less than 100 mW for high-quality videoconferencing on Smartphones and PDAs. The WirelessRay

configuration targets physical-layer processing for 802.11a, b, and g at less than 70 mW for wireless-LAN devices.

Addressing modes: The BOPS architecture supports SIMD (single-instruction-multiple data), MIMD (multiple-instruction-multiple-data) and SMIMD (synchronous-multiple-instruction-multiple-data) operation. A fully programmable, patternable, scalable DMA engine supports the addressing modes and data-flow management necessary to meet the computational requirements of the high-performance, scalable DSP cores.

Special instructions or integral-peripheral functions: Each family has an enhanced instruction set targeting mobile-wireless, mobile-video, or high-performance streaming media. You can easily integrate all functions—from a RISC coprocessor to a simple PCI interface—into BOPS SOCs (systems on chips).

Support: The BOPS software-development kit integrates tools for application-software programmers, SOC designers, firmware designers, and system architects into one development environment. The Jordan and Travis evaluation boards enable designers to evaluate the ManArray architecture and develop SOCs using the ManArray-based family of DSP cores. The BOPS Halo Parallelizing C-Compiler enables programmers to accelerate their software-development schedule by automatically exploiting the three levels of parallelism in the ManArray architecture, including packed data, processor arrays, and indirect VLIW (very-long-instruction word).

CHIPWRIGHTS CW4011, CW4511

at a glance:

- Devices can deliver 7500 MMACs (million MACs)/sec for less than 500 mW.
- The CW4511 includes peripherals targeting digital-camera applications.

The CW4011 visual-signal processor's high-performance, low-power architecture targets digital-signal-processing algorithms for imaging data that uses an SIMD/VDIW (single-instruction-multiple-data/very-dense-instruction-word) architecture and integrates eight parallel DSP-execution units and one RISC processor on the same die. Each DSP unit can generate its own address into memory to maintain processing throughput. The DSP array performs parallel accesses to the 128-kbyte, multibank SRAM through a 128-bit bus. The CW4011 normally acts as the system controller but can operate as a coprocessor that connects to many 8- and 16-bit microcontrollers. You can chain together multiple CW4011s through the integrated video ports for a distributed-multiprocessor system for image-processing applications.

The CW4511 builds on the CW4011 by adding I/O capabilities, such as USB, LCD outputs, and triple DACs for NTSC or PAL outputs, targeting digital-camera applications. The CW4511 lets you implement a digital camera, including image-processing algorithms, memory control, and other housekeeping functions with just one VLSI (very-large-scale-integration) chip. The CW4011 and CW4511 can achieve 7500 million MACs (multiply accumulates)/sec at power levels of less than 500 mW at full frequency. These processors can achieve CIF-level MPEG-4 encoding at more than 30 frames/sec, VGA-level encoding at more than 15 frames/sec, and JPEG compression at more than 20

million pixels/sec.

Addressing and processing modes: This processor family offers special addressing modes, including strided and scatter-gather memory accesses, supporting narrow data applications, such as imaging. Each parallel processor in the chip can perform arithmetic operations on one 32-bit, two 16-bit, or four 8-bit slices in one instruction.

Special instructions or integral-peripheral functions: This processor family includes special instructions for imaging, including a dot-product and a sum-of-absolute-differences instruction. The 16-bit video-in and -out ports with 256-byte FIFO buffers support simultaneous data transfers at 50M words/sec. The CW4511 includes integrated peripherals including a USB controller, an LCD output, and triple DACs for output NTSC or PAL video.

Development support: Metrowerks' (www.metrowerks.com) CodeWarrior integrated development environment supports development for the CW4011 and CW4511. These tools include an assembler, an ANSI C compiler, a linker, a simulator, and a profiler in an integrated, easy-to-use package. Because the user interface is identical to that of other products that CodeWarrior supports, engineers who have previously used CodeWarrior can immediately start using the ChipWrights version of this tool.

CIRRUS LOGIC CS494XX

at a glance:

- Support for AAC, DTS 96/24, and THX Cinema requires no additional external logic or memory.

Cirrus Logic's CS49400 DSP family integrates a front-end, 24-bit DSP for audio-standard decoding and a 32-bit, back-end DSP for PCM postprocessing. It features a dedicated multistandard decoder; key peripherals; and X, Y, and program memories in a single chip targeting digital-entertainment applications, such as audio-video receivers, outboard decoders, DVD receivers, DVD-audio/video/SACD (Super Audio CD) players, and automotive-entertainment systems. The device can support multichannel DTS 96/24, Dolby Digital, AAC, and THX Ultra2 Cinema without additional logic or memory, and it supports customer software-security keys.

Special instructions or integral-peripheral functions: Along with dual S/PDIF (Sony/Philips digital-interface) transmitters and serial and parallel host interfaces, the CS49400 includes eight-channel audio- input with PCM-output channels as large as 24 bits.

Development support: The CS49400 features an audio framework, including customizable programming, certified audio decoders, and sound-enhancement programs for DTS 96/24, Dolby Digital, AAC, and THX. Cirrus' software library provides legacy audio-decoder support.

CLARKSPUR CD2450 AND CD2480

at a glance:

- The CD2480 uses an open architecture to support additional instructions.

The configurable-processor CD2450 core has selectable datapath precision, register-set size, and interrupt structure. Memories may be on- and off-chip, ROM and RAM, and with different speeds and sizes. Peripheral-interface circuits support common functions and protocols, yet are configurable for the requirements of the application system. Clarkspur custom-designs all modules to fit together for a compact layout with minimum interconnection delays. All datapath elements are configurable to a precision of 16 to 24 bits. The multiplier is pipelined in two stages, producing a 31-bit product every 20 nsec with a latency of 40 nsec for new arguments in the X and Y registers. The ALU is full-function with double-word addition and subtraction with the 32-bit accumulator ACCH and ACCL. The shifter SHIFT covers a byte-wide range of left logical shifts and one of right arithmetic shifts on the b ALU input register.

The two data memories contain two sets of four address-pointer registers. You can index the pointers, which loop in arbitrarily sized buffers. One register in each set can act as a stack pointer for program instructions. The stack in RAM0 handles interrupts. The three interrupts are part of the system-function portion of the core. They have a three-level priority structure, and you can use them internally with interface modules or with external system signals. The user-defined two inputs and two outputs also handle system signals through noninterrupt programmed transfers.

The CD2480, an enhanced version of the CD2450, targets audio-compression applications in which extensive floating-point operations may take place, such as AAC, MP3, and CELP (Code Excited Linear Prediction). The core maintains a conventional 16-bit instruction-bit width but adds a 24-bit-data-width architecture, a strong barrel shifter, a normalizer/denormalizer, an enhanced RAM-pointer-modification capability, a double-loop-repeat instruction, a one-cycle-pipelined multiply and one-cycle operation in double-word instructions.

Addressing and processing modes: The CD2480 supports single- or double-word operation.

Special instructions or integral-peripheral functions: The core includes an optional Huffman Decoder instruction.

Development support: Clarkspur offers an assembler, linker, emulator, PC-based software debugger, and demo board. The emulator board on an FPGA runs only at low speeds (25 MIPS). Archelon (www.archelon.com) offers a META-C compiler that can use Clarkspur's code tables for software development.

DSP ARCHITECTURES DSP24

at a glance:

- The device targets low-power, software-minimized, frequency-domain signal-processing applications.
- Strategic radiation-hardened and high-reliability versions are available.

The high-performance DSP24 array-processor chip and its associated intellectual-property cores for signal and image processing in the frequency domain target applications that perform operations on large arrays of data. It is a pass-based processor, with each function valid for one complete pass. Each

operation code defines a basic flow for the desired operation that repeats for multiple pairs of data to complete one pass. For typical array-processing applications, such as FFTs, the device sets up a function code (for example, BFLY32). Radix32 butterfly then clocks the whole data array into the DSP24 and applies the function to the whole array. A latency occurs when you implement the DSP24 functions, for which the MMU24 automatically compensates when you use it in a system. The pipeline systolic structure allows you to cascade multiple DSP24s for increased performance and higher radices. This structure permits high-speed operation on an unlimited array size with support for enhanced read-only FFT, double-length FFT, dual FFT, and stacked FFT to reduce latency.

Addressing and processing modes: The DSP24 addressing includes digit reversing, read-only-FFT addressing, fast sine/cosine, decimation, interpolation, modulo increment/decrement, array padding, zero filling, radix2 through radix1024 patterns, and parameterized user sequences.

Special instructions or integral-peripheral functions: The DSP24 includes radix2 through radix1024 instructions, FIRs, and matrix multiplies. It can perform no-overhead window functions and filter/image multiplies and uses five bidirectional data ports for any-port-to-any-port data routing.

Development support: The DSP24 and optional MMU24 software-development kit come with C models and optional VHDL models. DSP Architectures offers the DSP24-EVM evaluation module. Valley Technologies (www.valleytech.com) offers board and module products, including the VectorWare language.

EQUATOR TECHNOLOGIES BSP-15 and MAP-CA

at a glance:

- Processor enables multiformat, high-definition decoding.
- Audio/video encoding/decoding engines support the processor.

The BSP-15 processor, a four-issue, superpipelined VLIW (very-long-instruction-word) architecture, includes four integer ALUs, two 64-bit SIMD ALUs, and two 128-bit SIMD (single-instruction-multiple-data) ALUs. The processor has 32 1-bit predicate registers, eight 128-bit registers, and 128 32-bit registers, which it can pair into 64-bit registers. The BSP-15 processor family targets video- and image-processing applications and is backward-compatible with Equator's MAP-CA chips. The BSP-15 supports as many as 50 billion operations/sec, 8 billion MACs/sec, 16 billion SAD (sum of absolute differences)/sec, and as many as six MPEG-2 D1 decodes.

The Equator MAP-CA BSP (broadband-signal-processor) chip is 100% programmable in C and targets consumer applications. The VLIW core includes four execution units on two clusters for VLIW parallel processing at the instruction level, native SIMD operations, four-way-set-associative, nonblocking write-back data cache, and a two-way-set-associative instruction cache. The MAP-CA chip can perform 30 billion operations per second while running common media-processing tasks, such as motion estimation. Equator designed the MAP-CA processor to operate at a core voltage of 1.8V with I/O signals of 3.3V. Depending on processor speed and application, the MAP-CA processor dissipates 2.5 to 6W of power. The MAP-CA processor is available in a 352-pin BGA package.

The processor stores instructions in a compressed format and presents them to the VLIW processor via 32-kbyte, two-way set-associative instruction cache with an LRU (least recently used)-replacement policy. It presents data to the processor by a 32-kbyte, four-way set-associative, four-bank-interleaved data cache using an LRU-replacement policy. Separate instruction, data, and DMA MMUs, each with a fully set-associative, 16-entry TLBs (translation look-aside buffers), provide memory protection. Off-chip memory connects via a glueless 64-bit SDRAM/SGRAM interface supporting as much as 128 Mbytes of external memory. The BSP processor family is 100% C/C++ programmable, allowing designers to port new and evolving video-compression algorithms to the BSP-15 processor platform, using Equator's optimizing compilers. A single BSP-15 chip can replace multiple fixed-function devices, such as hardwired-MPEG chips.

The variable-length encoder/decoder coprocessor with 4-kbyte instruction and 4-kbyte data memories offloads bit-serial tasks from the VLIW core and handles variable-length encoding and decoding. The video-filter coprocessor, aided by a 6-kbyte line buffer, provides as many as four vertical-tap and five horizontal-tap filters. The DataStreamer, a programmable, 64-channel DMA controller with 8 kbytes of buffering, provides high data throughput. The display-refresh controller provides color-space conversion, palette-table look-up, and hardware-cursor functions. A DES coprocessor accelerates DES encryption and decryption.

Special instructions or integral-peripheral functions Specialized video instructions provide video acceleration, and specialized audio instructions enable efficient mapping. The programmable format, 64/32-bit SDRAM controller requires no additional glue logic. The PCI bus is compatible with 3.3V, 33/66-MHz, 32-bit, PCI Revision 2.2 and includes an internal host arbitrator. Integrated peripheral interfaces include a IIC (inter-IC) serial-I/O-bus-control port, flash-ROM controller, S/PDIF (IEC958) and IIS serial-audio I/O ports, an 8-bit ITU-T BT.656 video-encoder-output port, and control signals for an external-video VCXO timing-control loop for MPEG transport-clock recovery. The programmable SVGA-display refresh controller provides 24-bit (8 bits times three), 135-MHz digital-to-analog conversion. The device also includes two multipurpose ports, each of which can function as an ITU-R BT.656 video-decoder-input port or a transport-channel-interface port.

Development support: Version 6.0 of Equator's iMMediaTools software-development tool kit allows designers to develop and deploy videocentric applications with the BSP-15 chip running Linux. Equator and its software partners offer a range of video and codecs, including MPEG-2, MPEG-4, H.263, H.264, MJPEG, Windows Media 9 Series, RealVideo9, DivX, MP3, AC3, AAC, and other proprietary, low-bit-rate, streaming-video codecs. They also offer reference designs for digital-security and surveillance applications, including digital-video-recorder, IP-camera, motion-detection, motion-tracking, biometrics, and camera-steadying applications.

The Tetra hardware platform supports rapid prototyping with a BSP processor targeting IP smart cameras, digital-video recorders, or IP-based Internet streaming-video applications. The modular design includes the Tetra CPU board, an open peripheral interface for add-on modules, and add-on "personality" modules. The Tetra CPU board measures 2.75×4 in., supporting hardware-reference designs for small-footprint applications.

The broadband video-on-demand reference platform, for low-bit-rate video-on-demand systems with Internet access and content security, provides less than 1 mbps with DVD-quality video. The multiformat, high-definition DVD player/recorder reference design can support popular film, Internet, and DVD-video formats, including Microsoft Windows Media 9 Series, encoding and decoding at

standard and high definition.

EVATRONIX C32025TX

at a glance:

- The C32025TX architecture is four times faster than the original architecture at the same clock speed.
- Most instructions support repeat mode.

The C32025TX, a three-stage-pipelined, 16-bit, fixed-point DSP core, implements the same instruction set as Texas Instruments' TMS32025 and provides the same interrupts, serial interface, and timer and executes most of instructions in a single clock time. The C32025TX is a microcode-free design targeting ASIC and FPGA implementations that avoids internal tristates and is strictly synchronous with both-edge clocking and synchronous reset. The C32025TX implements a Harvard-type architecture, maintaining two separate program- and data buses for full-speed execution. The program bus carries instructions and immediate operands; the data bus interconnects various components and carries data between any data- memory space. Both buses can carry data for single-clock MAC operations.

Addressing and processing modes: The C32025TX supports memory-direct, indirect, and immediate addressing modes. Direct mode uses a 9-bit page pointer and the seven least significant bits of the instruction word. Indirect mode and operations with reversed-carry propagation use 8×16-bit registers and a 16-bit auxiliary-register arithmetic unit. Immediate addressing mode uses a 16-bit-long-instruction immediately following the instruction word.

Special instructions or integral-peripheral functions: The instruction set and control signals support block memory transfers, communication to slower off-chip devices, and multiprocessing implementations. Most instructions support repeat mode for block moves, MAC (multiply-accumulates operations, I/O transfers, and table reads and writes. The C32025TX includes single-clock MAC instructions, two large on-chip RAM blocks, eight auxiliary registers with dedicated arithmetic unit, a serial interface, and a hardware timer. The C32025TX has a 16-bit reload timer and a synchronous serial port for a direct codec interface.

EVATRONIX C56000

at a glance:

- Core delivers 80 MIPS when you implement it in a 0.18-micron process (160 MHz).
- Two parallel moves are possible in one instruction cycle.

The C56000 is a three-stage-pipelined, 24-bit, fixed-point DSP core. The efficient modified-Harvard architecture provides high precision and performance using independent X/Y-memory accesses. The C56000 implements the same instruction set and provides the same peripherals and interrupts as the industry-standard DSP56002. The architecture maximizes processing power by maintaining separate two-data and one-program buses for full-speed execution. Two clock-cycle arithmetical instructions,

three on-chip RAM blocks, an address-generation unit with 24 dedicated registers, two full-duplex serial interfaces, a hardware timer, and a host interface make the processor appropriate for data-intensive signal processing. The address-generation unit, program-control unit, ALU; memory; and peripheral block operate independently of and in parallel with the other units using a sophisticated bus system. Instruction prefetch, 24×24-bit multiplication, 56-bit addition, two data moves, and two address-pointer updates can execute in one instruction cycle.

Addressing and processing modes: The C56000 DSP has eight sets of three 16-bit registers: address, offset, and modifier. It supports direct, indirect, and immediate addressing modes and has varied indirect-addressing modes using linear, modulo, and reverse-carry arithmetic. It executes two 16-bit address calculations every instruction cycle for the program and X/Y data-memory spaces.

Special instructions or integral-peripheral functions Most arithmetic instructions of C56000 use parallel moves. The core supports nested loops and can repeat one instruction or a block of instructions a set number of times. It performs single-cycle MAC (multiply-accumulate) instructions with rounding. The SCI and SSI ports support direct codec interfacing, and 24 general-purpose-I/O pins, in parallel with the 24-bit timer, enable the DSP to work as a microcontroller.

Development support: These DSP cores are compatible with instruction-set architectures of once widely used chips, which Texas Instruments and Motorola made obsolete; therefore, designers may develop software for these cores with any compiler and assembler that generate code for those architectures. Some cores include First Silicon Systems' (www.fs2.com) on-chip instrumentation. The on-chip-debugging-support module, a JTAG-accessible plug-in, can control the processor (modify any register, execute any instruction and run it in step mode) and set breakpoints on any instruction or data. Signum Systems' (www.signum.com) in-circuit emulator supports debugging as fast as 100 MHz for the R80515 and features real trace mode and real-time visibility into the memory and registers.

HITACHI SEMICONDUCTOR SH-DSP AND SH3-DSP

at a glance:

- The SH7622 can perform 130 MIPS at 100 MHz.
- The SH7727 can perform 208 MIPS at 160 MHz.

Processors in the SH-DSP series (SH7616, SH7622, and SH7065) combine a 32-bit RISC CPU and a 16-bit integer DSP unit into a single core. The DSP unit can execute single-cycle, 16×16-integer multiplies and multitask its operations. Hitachi's SH7616 is a CMOS single-chip microcontroller that integrates a 10/100-Mbps Ethernet controller supported by two 2-kbyte FIFOs and a multichannel DMA controller targeting Ethernet applications, such as network video/printers, network terminals, and management processors. The SH7065 integrates 256 kbytes of on-chip flash.

Processors in the SH3-DSP series (SH7727, SH7729R) combine a 32-bit RISC CPU and 16-bit integer DSP unit into a multitasking core with a four-bus structure targeting Web/Smartphone, handheld-PC, Internet-terminal/IP-fax, digital-still-camera, and security-terminal applications. SH3-DSP devices include 16 kbytes of X/Y RAM, 16-kbytes of cache (ways 2 and 3 lockable), a bus-state controller for glueless connection to SDRAM, and on-chip JTAG and real-time instruction-trace-debugging modules.

The SH7729R includes data protection and virtual memory.

Addressing modes: These devices support direct- and indirect-register, predecrement or postincrement indirect-register, indirect-register-with-displacement, indirect-indexed-register, indirect-global-base-register-with-displacement, indirect-indexed-global-base-register, indirect-program-counter-with-displacement, and program-counter-relative immediate addressing.

Special instructions or integral-peripheral functions:The SHDSP and SH3-DSP use a 16- and 32-bit instruction set that supports one-cycle multiplication/addition, operand-unrelated parallel moves, conditional execution for DSP datapath instructions, multiprecision arithmetic in microcontroller instructions, and single-cycle exponent detection. (DSP operations are all 32-bit instructions.)

The SH7622 SH-DSP core device includes high-speed on-chip USB. SH3-DSP devices include a memory-management unit, a timer, a real-time clock, an interrupt controller, and a serial-communication interface. The SH7727 includes USB host and LCD controllers that support bus-master functions. The SH7729R includes infrared communication, an ADC, a DAC, and power management.

Support: Hitachi and third parties offer evaluation kits, emulators, companion chips, reference-design platforms, software board support, RTOSs, middleware, and application packages. Hitachi offers middleware for the SH-DSP and SH3-DSP covering telephony applications, including G.729, G.725, and G.723.

HYPERSTONE E1-16XSR AND E1-32XSR

at a glance:

- A single-core RISC/DSP suits battery-driven multimedia devices.
- Core gate count is 35,000 without RAM.

Hyperstone E1-32XSR is a single-core RISC/DSP targeting digital-still-camera applications. All of the instructions, including the DSP instructions, use RISC principles. Parallelism exists between the ALU, the DSP, and the load/store units. Hyperstone implements the core as a static design, and it can operate as fast as 220 MHz with a current consumption of 40 mA. The architecture includes SDRAM, EDO RAM, flash memory, I/O-bus interfaces, on-chip PLL, 16 kbytes of SRAM, and a timer. Variations are available on request. The bus interface provides four external memory areas, each 1 Gbyte in size with individual bus width and bus timing. You can control the on-chip PLL via software, making possible a speed variation by a factor of as much as 16 within one clock cycle.

Addressing and processing modes: The core bases all instructions on the load/store principle that RISC processors use. It supports subword processing, a kind of “lean VLIW (very-long-instruction-word)” principle.

Development support: Windows-and Linux-based system-development tools are available. Embedded Linux is the supported operating system. A network of partners offers services and capabilities, including ASIC design and Bluetooth IP.

IMPROV SYSTEMS JAZZ

at a glance:

- Direct on-chip data memories handle processor-to-processor data communication.
- All processors attach to a single Q-Bus that enables queuing of tasks.

The Jazz DSP configurable, VLIW (very-long-instruction-word) architecture incorporates overlaid datapaths, a distributed register system, code compression, and power management. The architecture allows designers to customize the computational resources and instruction set of the processor. Designers can customize the Jazz PSA (programmable-system architecture) to optimize key application algorithms. The Jazz PSA defines a processing platform comprising multiple Jazz processors, nonvolatile instruction memory, configurable I/O interfaces, and hardware support for u-tasking. The DSP-core architecture facilitates rapid design modifications without compromising the verification integrity and tool chain of the processor. The Jazz PSA can scale from a single Jazz DSP core to a system-level platform implementation that many unique processors in an interconnect structure. The orthogonal memory structure enables the device to independently map, address, and configure the instruction and data-memory spaces for width and size.

Addressing and processing modes: Supported standard addressing modes include direct, indirect, indexed, immediate, displacement, bit reverse, bit-reverse index, vector index, and postincrement. A wrap mode supports circular buffers.

Special instructions or integral-peripheral functions Special instructions support single-cycle built-in library functions for common signal-processing data transforms, and a set of task control instructions supports the unique u-task scheduling in the PSA.

Development support: The Jazz DSP supports a flexible design methodology that customizes the computational resources and instruction set of the processor. The development-tool chain includes an IDE, a compiler, an assembler, an instruction-set simulator, a profiler, a debugger, and FPGA-emulation support. The Jazz PSA Composer tool suite supports processor customization in a graphical design environment. The Jazz PSA standard tool suite supports programming for unique processor configurations so that designers do not need custom programming tools.

Improv's Rehearsal boards provide a near-real-time system for designers to run configurations of the Jazz PSA core and to verify that designer-defined DSPs run with other elements of the overall system. Improv offers platform solution kits that are a collection of hardware and software components, such as custom Jazz DSPs, application software, and reference designs, targeting application-oriented SOC (system-on-chip) development. Acappella is a family of application-optimized hardware and software targeting voice-over-packet applications. To better meet the needs of resource-constrained designs, Easy Jazz kits offer suites of application software, hardware-integration blocks, and verification code.

LSI LOGIC ZSP400, LSI402ZX, AND LSI403LP

at a glance:

- Dual add-compare-select operations in one cycle support efficient Viterbi decoding.

The ZSP400, a dual-MAC (multiply-accumulate) unit, four-issue superscalar processor architecture, uses a 16-bit instruction set with dual 16-bit arithmetic operations that you can combine to provide a high-precision, 32×32-bit single-cycle multiply and add to support high-resolution audio and multimedia applications. The ZSP400 implements a five-stage, four-way superscalar pipeline to process as many as 20 instructions at a time. The processor's execution unit contains two ALUs.

The LSI402ZX is a high-performance, 16-bit, fixed-point DSP core targeting voice-over-network CPE/IAD (customer- premises-equipment/integrated-access-device) devices, infrastructure, wireless-infrastructure, and audio applications. The LSI402ZX includes 62k words of instruction RAM and 62k words of data RAM. The LSI403LP is a low-power, 16-bit, fixed-point DSP core targeting voice-over-network CPE/IAD devices and audio applications. The LSI403LP provides 16k words of instruction RAM, 16k words of data RAM, and 16k words of instruction- or data-configurable memory. An eight-channel DMA controller, which transfers instructions or data to and from memory, supports both devices.

Addressing and processing modes: The ZSP400 provides two independently enabled circular buffers and supports reverse-carry addressing. Reverse-carry addressing is an alternative mode of indexing the base-address registers that speeds FFT and similar operations that require modification of the next-load or -store address in a reverse-carry fashion.

Special instructions or integral-peripheral functions: The ZSP400 can perform a single-cycle add-compare-select for efficient Viterbi decoding. It also supports bit manipulation, 32-bit arithmetic, logic operations, and two-cycle complex-multiply instructions. The LSI402ZX and LSI403LP include two high-speed TDM serial ports, an 8-bit (LSI403LP) or 16-bit (LSI402ZX) host-interface port, an external memory-interface unit, a four-pin (LSI403LP) or an eight-pin (LSI402ZX) programmable I/O port, and an IEEE 1149.1 JTAG port for program downloading and debugging.

LSI LOGIC ZSP500

at a glance:

- Power-management controls dynamically switch execution units on or off based upon program usage.
- Designers can extend the instruction set by as many as 256 customer instructions.

The ZSP500, a low-power, high-performance, dual-MAC (multiply-accumulate) unit, quad-issue superscalar processor architecture, has an instruction set rich with DSP capabilities. The ZSP500 uses a 16- and 32-bit instruction set with dual 16-bit arithmetic operations that you can combine to provide a high-precision, 32×32-bit, single-cycle multiply and add supporting high-resolution audio and multimedia applications. The ZSP500 implements an eight-stage, four-way-superscalar pipeline to process as many as 32 instructions at a time. The processor's execution unit contains two MAC units, two general-purpose ALUs and two dedicated ALUs for address generation. The LSI500P is a silicon prototyping vehicle that incorporates the ZSP500 core, the memory subsystem, 256k words of SRAM, and an integrated AMBA/AHB interface with the AMBA I/O pins available off-chip as well as

complete pin access to the coprocessor port.

Addressing and processing modes: The ZSP500 provides for both Harvard and unified memory-addressing schemes. The ZSP500 supports a range of indexed and bit-reversal addressing. Reverse-carry addressing is an alternative mode of indexing the base-address registers that speed FFT and similar operations that require modification of the next-load or -store address in a reverse-carry fashion.

Special instructions or integral-peripheral functions: The ZSP500 includes a coprocessor interface that allows designers to add as many as 256 tightly coupled custom instructions to the processor without affecting the processor baseline datapaths. The ZSP500 core includes a memory subsystem that is configurable for data- and instruction-memory sizes from 4k to 128k words per block. The ZSP500 comes with an ARM ABMA/AHB interface bridge and a reference system with sample AMBA/AHB peripherals.

LSI LOGIC ZSP600

at a glance:

- Three add-compare-select operations in one cycle support efficient Viterbi decoding.
- Designers can extend the instruction set by as many as 256 customer instructions.

The ZSP600, a high-performance, quad-MAC (multiply-accumulate)-unit, six-issue superscalar processor architecture, uses a 16- and 32-bit instruction set with dual 16-bit arithmetic operations. You can combine these operations to provide a dual, high-precision, 32×32-bit single-cycle multiply and add that is necessary for high-resolution audio and multimedia applications. The ZSP600 implements an eight-stage, six-way-superscalar pipeline to process as many as 48 instructions at a time. The processor's execution unit contains four MAC units, four general-purpose ALUs, and two ALUs dedicated to address generation. The ZSP600 features dual independent 64-bit load/store ports, providing as much as 6.4 Gbytes/sec of I/O.

Addressing and processing modes: The ZSP600 provides for both Harvard and unified memory-addressing schemes. The ZSP600 supports a wide range of indexed and bit-reversal addressing support. Reverse-carry addressing is an alternative mode of indexing the base-address registers that speed FFT and similar operations that require modification of the next-load or next-store address in a reverse-carry fashion.

Special instructions or integral-peripheral functions: The ZSP600 includes a coprocessor interface that allows designers to add as many as 256 tightly coupled custom instructions to the processor without affecting the processor baseline datapaths. The ZSP600 core comes with a memory subsystem that is configurable for data and instruction memory, from 4k to 128k words per block. The ZSP600 comes with an ARM ABMA/AHB interface bridge and a reference system with sample AMBA/AHB peripherals.

Development support: LSI delivers all three licensable core-product offerings in a technology-transfer package that includes Verilog RTL source code; scripts for Design Compiler, Physical Compiler, or

both, as well as static-timing-analysis scripts for Primetime; and a verification suite to test implementations for correct construction, as well as an example system to provide an out-of-the-box system as a reference. Designers can tune these scripts to vary the gate count, die size, clock speed, and power dissipation of all three core offerings for tailoring to an application's requirements. These core-product technologies incorporate AMBA interfaces to allow a glueless interface to ARM-based microprocessor designs. The ZSP500 and ZSP600 have extended debugging support to include on-core profiling, ETM (Embedded Trace Module), and real-time hardware trace. Each core includes documentation, such as the ZSP Architecture for Programmers, the Core User's Guide for system designers, and a VLSI Implementation Guide for chip designers.

LSI provides an integrated ZSP software-development kit that supports all three processor cores and includes an optimizing C compiler, an assembly optimizer, a linker, an assembler, cycle- and instruction-accurate simulators, and a debugger with advanced features, such as a pipeline viewer and instruction-grouping analyzer. The software-development kit incorporates a library of commonly used DSP-function calls and supports development on both Windows and SPARC Solaris platforms. The cycle-accurate simulator can serve as a DLL to link to larger simulation-model environments, and designers can add their own models for custom peripherals. LSI Logic has combined the cycle-accurate simulator with a bus-interface model to provide a mixed-mode simulation capability in VCS/ModelTec environments.

Corelis (www.corelis.com), Macraigor Systems (www.macraigor.com), and Green Hills Software (www.ghs.com) offer a variety of JTAG probes. Third-party modeling support of the ZSP includes a kit for Cadence's (www.cadence.com) Signal Processing Workstation on the ZSP400 and a processor-support kit for Mentor Graphic's (www.mentor.com) Seamless co-verification tools for all three DSP cores. Green Hills Software offers the Multi software-development tool chain, which includes an optimizing C compiler, an assembler, a linker, a cycle-accurate simulator, a debugger suite, and additional features for project building and code balancing. It can interface with Matlab for data visualization and multicore debugging in a heterogeneous processor environment that can include ZSP, ARM, MIPS, and PowerPC processors. The multiprocessor core-debugger support operates from a single JTAG interconnection, supporting low-pin-count interfaces for SOC (system-on-chip) designs.

LSI offers royalty-free source-code licenses of production- grade, assembly-optimized ZSP application software for audio, multimedia, and wireless markets. These modules comply with LSI Logic's open-architecture ZOpen Software Framework, a royalty-free, C-source-code product that provides integration guidelines, supporting utilities and a methodology that standardizes application development. ZSP software-application partners provide ZOpen-compliant algorithms. Optional real-time operating systems are available, including those from OSE Systems (www.ose.com); Micrium U-COS (www.micrium.com); and Express Logic (www.expresslogic.com), which provides Thread-X support for ZSP cores.

MOTOROLA DSP56800 AND DSP56800E

at a glance:

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Motorola's DSP56800 family integrates the instruction set of a DSP with the control functions of an embedded microcontroller into a single core. The 56800 family of products targets applications that traditionally use 16-bit microcontrollers but also require DSP functions, such as point of sale, voice recognition, digital telephone-answering devices, motor-control systems, and applications requiring voice, audio, or data processing. Motorola's 56800E family enhances the DSP56800 architecture by providing five times the performance (to 200 MIPS) at one-third the power consumption of the original core, and by doubling code density. It offers expanded memory addressing for as much as 4 Mbytes of program memory and 32 Mbytes of data memory. The 56800E includes 19 addressing modes and 8-, 16-, and 32-bit data types; supports fast interrupts; and supports real-time debugging.

The 56F83X flash-based DSP controllers use 60 MHz and 60 MIPS, have embedded flash memory, and support an extended temperature range of -40 to $+125^{\circ}\text{C}$. The 56F83x family of devices targets automotive, instrumentation, and industrial-networking applications, including electronic power-assisted steering, data-acquisition equipment, and factory-automation systems.

Addressing and processing modes: The address-generation unit performs all address calculations to minimize execution time. Addressing modes specify the location of the operands—whether they are immediate values, in a register, or in memory—and provide the exact address of the operands. The architecture groups 19 addressing modes into register-direct, address-register-indirect, immediate, and absolute categories. The 56F83x family also supports parallel-instruction execution.

Special instructions or integral-peripheral functions: The 56800 includes a bus structure that allows it to move data at the speed of the DSP and offers the peripheral set of a microcontroller, such as an interrupt controller, an external memory interface, general-purpose I/O, a scalable controller-area network, ADC, a quadrature decoder, a pulse-width modulator, SCI, SSI, SPI, a quad timer module, and on-chip-emulation.

Development support: The Metrowerks (www.metrowerks.com) CodeWarrior IDE tool set supports software development across Motorola's entire family of 16-bit controllers. It includes an optimized C compiler, an assembler, a linker, a debugger, and an instruction-set simulator. Motorola offers target development boards and companion daughtercards for market-specific applications, such as motor control, industrial, and automotive. Other third-party tool developers and consultants support 56800 devices.

NEC ELECTRONICS SPXK5

at a glance:

- SPXK5 achieves 1000 MIPS/500 MMACs (million MACs) at 250 MHz.
- Enhanced media instructions accelerate video codecs.

The SPXK5, a four-way VLIW (very-long-instruction-word) DSP core, has a highly orthogonal instruction set that enables efficient high-level-language code generation and features low-power consumption. It targets multimedia applications on handheld terminals, such as 3G mobile phones and PDAs. The SPXK5 contains seven functional units, two 32-bit data buses, one 64-bit instruction bus, and register files. The functional units comprise two MAC (multiply-accumulate) units for 16×16 -bit

multiplication and 40/16-bit accumulation; two ALUs for addition/subtraction, shift, and logical operations; two data-address units for load and store; and one system-control unit for branch, zero-overhead looping, and conditional execution. The SPXK5's register files include eight general-purpose, 40-bit registers, eight address registers, eight corresponding offset registers, and other system registers. The SPXK5 can issue as many as four instructions in parallel during the same clock cycle, as long as the total length of the instructions does not exceed 64 bits. All arithmetic, logical, and load/store operations other than MAC operations are single-cycle operations.

Addressing and processing modes: The SPXK5 core architecture supports direct-addressing mode, postmodify-indirect addressing mode, and premodify-indirect-addressing mode. The postmodification operations available for the address registers include no change, increment, decrement, index addition, modulo index addition, and bit-reversed.

Special instructions or integral-peripheral functions Eight application-specific instructions support image/video processing and Viterbi decoding and provide sufficient coverage without significantly increasing the length of instruction encoding fields or the total code size. The PADD, PSUB, PSHIFT, PADDABS, PACKV, UNPACKV instructions are effective for the core functions of a video encoder/decoder algorithm. These instructions can accelerate MPEG-4 video-codec performance by 20%. The add-compare-select operation is the core of the Viterbi decoding. The SPXK5 can execute the PADD, PSUB, and PMAX instructions in two cycles and complete two ACS operations.

Development support: NEC Electronics provides GUI-based software-development tools for SPXK5 that include an ISO/ANSI-C compiler, an assembler/linker, a simulator, and a source-level debugger. The compiler provides enhanced optimization, such as instruction scheduling, inlining, loop analysis, and machine-dependent tuning. For efficient target code, the compiler accepts programs in DSP-C—a language extension of ISO-C including key DSP features, such as fixed-point types.

OAK TECHNOLOGY PM-44IX

at a glance:

- The four parallel-pipelined processors can perform 3700 MIPS/930 MMACs (million MACs) at 233 MHz.
- The PM-44ix supports as many as 16 color-ink-jet and 30 monochrome laser copies per minute.

Oak Technology's iDSP family targets image-processing applications, such as imaging-enabled printers and multifunction peripherals. The iDSP provides designers with the flexibility of a software-based image-processing option. The PM-44ix contains four symmetric parallel-pipelined processors and employs the SIMD (single-instruction-multiple-data) parallel-processing architecture to take advantage of the parallelism inherent in image data.

Addressing and processing modes: All memory accesses in the iDSP are 32 bits wide.

Special instructions or integral-peripheral functions Special extraction and insertion units allow designers to manipulate bit fields of any size within 32-bit registers. The iDSP instruction set contains specialized instructions for coordinating parallel processing.

Development support: The iDSP programming environment includes an IDE, an image-processing library, and an evaluation board. Oak Technology's worldwide direct sales and support organization supports the iDSP.

PARTHUSCEVA OAKDSPCORE

at a glance:

- The OakDSPCore handles bit-manipulation, control, and DSP instructions.
- Power management includes active, slow, and idle modes.

The 16-bit, four-stage-pipeline, fixed-point, single-MAC, licensable OakDSPCore architecture includes DSP and microcontroller instructions for higher code density. It is the second member of the SmartCores family. The OakDSPCore has two data buses and one program bus, configurable ROM/RAM size, a data-address-arithmetic unit, a multiplier, a 36-bit ALU, two sets of two 36-bit accumulators, and support for a C++/C-compiler. It includes a bit-manipulation unit with a 36-bit barrel shifter, an exponent-evaluation unit that supports fast normalization, and a bit-field-operation unit. The zero-

overhead-loop mechanisms include an interruptible single-word instruction loop and four-level nesting of block repeats. User-definable registers speed hardware acceleration and provide coprocessor support. It has single-cycle interrupt latency and automatic context switching. Power management includes active-, slow-, and idle-operation modes. OakDSPCore is compatible with the PineDSPCore.

Addressing and processing modes: The OakDSPCore supports register, single and double-indirect, short- and long-immediate, short- and long index, and stack-pointer addressing modes. It supports circular (modulo) buffering for all its pointers and direct addressing for the entire 64k-word data space. It also has a program-memory-indirect addressing mode.

Special instructions or integral-peripheral functions: The OakDSPCore handles bit-manipulation, control, and DSP instructions. Instructions include single-cycle minimum/maximum calculation with pointer latching, double-precision calculations, normalization, exponent, conditional accumulator modifications, division step, read-modify (add/subtract/OR/AND/XOR)-write, test 16-bit mask bits and test bit, delayed return, interruptible single-word repeat loop and block repeat, 36-bit shift left or right in a single cycle, and a bank exchange of alternative registers.

PARTHUSCEVA PALMDSPCORE

at a glance:

- Seven arithmetic units support SIMD and MIMD instructions.
- Core offers parallelism using 16- and 32-bit-wide instruction.

PalmDSPCore is a family of three licensable, highly parallel, and dual-MAC soft DSP cores—of 16, 20, and 24 bits—targeting 2.5 and 3G terminals, voice-over-IP gateways, streaming audio/video, and infrastructure applications. PalmDSPCore is an instruction-level-parallelism architecture including

MIMD (multiple-instruction-multiple-data) and SIMD (single-instruction-multiple-data) instructions are seven computation units working in parallel. The symmetrical cross-coupled MAC (multiply-accumulate) paths allow non-FIR-oriented algorithms, such as complex Radix-2 FFT butterfly, to execute in two cycles. PalmDSPCore has internal mechanisms and special instructions to reduce power consumption, in addition to active, slow, and idle power-management modes. PalmDSPCore has two multipliers; a three input ALU; a three-input split adder-subtractor unit; four orthogonal, 40/48/56-bit accumulators; and a bit-manipulation unit. The data-address arithmetic unit contains two additional adder-subtractor-units, which can perform control functions in parallel to the arithmetic calculations at the computation and bit-manipulation unit. It has zero-overhead-loop mechanisms with infinite levels of repeat and block repeat and six pipeline stages. PalmDSPCore increases code density by using variable instruction width (16 or 32 bits) so that a complete N-taps FIR filter is coded in only four words and executes in $N/2+1$ cycles. You can extend program memory to 32 Mbytes. PalmDSPCore is a process- and library-independent, fully synthesizable soft core, compatible with previous SmartCores generations, including Teak, TeakLite, and OakDSPCore.

Addressing and processing modes: PalmDSPCore supports circular buffering, register, short- and long-direct, short- and long-immediate, relative, bit-reversal, double-word, parallel, index-based, conditional, and stack-pointer addressing. It also supports quadruple indirect addressing mode to simultaneously feed four inputs of the two multipliers or four inputs of the split ALU.

Special instructions or integral-peripheral functions PalmDSPCore has single, parallel, and multiparallel instruction sets that include SIMD and MIMD instructions. The core can execute as many as 18 operations in a single cycle using a 16- or 32-bit instruction width. It supports DSP and microcontroller instructions such as dual-MAC, complex FFT butterfly in two cycles, Viterbi decoding in two cycles, vector quantization, delayed branches/return, normalization, exponent, conditional instructions (parallel moves, logic, arithmetic, and accumulator), single-cycle 40/48/56-bit shift left/right bit-field and insert-extract operations. For accelerating specific tasks, you can further extend the core with as many as 16 custom accelerators.

PARTHUSCEVA PINEDSPCORE

at a glance:

- The DSP-and-control instruction set is compact.
- PineDSPCore is a licensable DSP core.

PineDSPCore, the first generation of the SmartCores family, is a 16-bit, fixed-point, single-MAC (multiply-accumulate) unit, licensable DSP core. It has a compact DSP-and-control instruction set for high code density. PineDSPCore has two data buses and one program bus, a configurable ROM/RAM size, and a data-arithmetic-addressing unit. The computation unit includes a multiplier; a 32-bit product register; a 36-bit ALU; two 36-bit accumulators, including four guard bits; and a normalization mechanism. The ALU performs arithmetic and logic operations, such as step division and rounding. PineDSPCore includes two zero-overhead loop mechanisms: a single-word instruction loop and a block repeat. It has user-definable registers for hardware acceleration, coprocessor support, or both. It has three pipeline stages and single-cycle interrupt latency. Power management includes active-, slow-, and idle-operation modes.

Addressing and processing modes: PineDSPCore supports register, single- and double-indirect, and short- and long-immediate addressing modes. It has a program-memory indirect-addressing mode and supports circular (modulo) buffering for all its pointers and direct addressing for the entire 64k-word data space.

Special instructions or integral-peripheral functions: Instructions include conditional accumulator modifications, conditional and unconditional call and branch, arithmetic and logical operations, round, rotate, shift, compare, division step, MAC, square, single-word repeat loop, and block repeat.

PARTHUSCEVA TEAK AND XPERTTEAK

at a glance:

- All instructions are 16 bits wide, including dual-MAC instructions.
- Teak handles complex FFT in five cycles and Viterbi decoder in three cycles.

The fully synthesizable, low-power, 16-bit, fixed-point, dual-MAC (multiply-accumulate) unit, licensable Teak DSP soft core has an instruction-level-parallelism capability. It targets cellular terminal digital cameras, voice-over-IP gateways and Internet-audio applications. Teak has active, slow, and idle power-management modes in addition to internal mechanisms to reduce power consumption. Teak includes a configurable memory size; a data-address-arithmetic unit; two multipliers; a 40-bit, three-input, split ALU; four 40-bit accumulators; an exponent unit; and a bit-manipulation unit. It has integrated accelerators for complex FFT; Viterbi-decoder; RTOS; and bit-exact standards, such as GSM communications. It has zero-overhead- loop mechanisms with infinite levels of repeat and block repeat, vectored interrupt, small interrupt latency, and wide-automatic-context-switching. Designers can extend Teak's program memory to 8 Mbytes and the core by hardware accelerations via the user-definable registers. Teak is code-compatible with the OakDSPCore and TeakLite instruction sets of SmartCores.

The XpertTeak is a fully synthesizable, process-independent, licensable option of a low-power, programmable-DSP core, targeting cellular, image, video, audio, speech, and voice-over-packet applications. XpertTeak is available as a stand-alone DSP SOC (system on chip) or embedded with an ARM SOC. The embedded offering includes an AMBA bridge and an APB bridge. XpertTeak is based on the dual-MAC Teak DSP core with the addition of a high-performance DMA controller, buffered time-division-multiplexing ports, a host-processor interface, and timers. The power-management unit can reduce the power consumption of inactive peripherals.

Addressing and processing modes: Teak supports circular (modulo) buffering, register, short- and long-direct, short- and long-immediate, relative, bit-reversal, and short- and long-index-based addressing modes. It can also perform quadruple-indirect addressing (for example, to simultaneously feed four inputs of the two multipliers or four inputs of the split ALU). The XpertTeak has separate instruction- and data-memory ranges. It can access as much as 8 Mbytes of program memory and 8 Gbytes of data memory. It incorporates a synchronous SRAM interface for the memories.

Special instructions or integral-peripheral functions: Instructions include dual-MAC operation, read/write double words to and from memory, and single-cycle minimum/maximum search with pointer latching. Teak handles complex FFT butterfly in five cycles and Viterbi decoding in three cycles. It

includes bit-manipulation and microcontroller instructions, double-precision multiplication, normalization, single-cycle exponent evaluation, conditional instructions, coprocessor support, division step, and infinite levels of repeat and block repeat. All the instructions are 16 bits wide, supporting compact code. Teak supports cycle stealing and burst-mode DMA, program boot, and code downloading.

XpertTeak includes an eight-channel DMA controller, two buffered time-division multiplexing ports, a 8/16-bit host port that facilitates interfacing to a variety of host processors in the stand-alone offering or AMBA and APB bridge in the embedded offering. XpertTeak also includes a power-management unit, serial I/O, a vectored interrupt-control unit, timers, PWM generators, JTAG, and an on-chip-emulation-module.

PARTHUSCEVA TEAKLITE AND VOPSTREAM

at a glance:

- TeakLite is a low-power-consumption, licensable core.
- VoPStream is a licensable design for voice-over-packet applications.

The 16-bit, fixed-point, single-MAC (multiply-accumulate)- unit, licensable TeakLite soft DSP core is code-compatible with the OakDSPCore instruction set. It enhances the OakDSPCore in portability, frequency, power consumption, and area. It is a process- and library-independent soft core, increases operating speed by 30% in the same process technology, and reduces power consumption by architecture and power-reduction mechanisms. Its design methodology better meets ASIC-design-environment requirements by employing a single-edge design (still with four pipeline stages) and full or partial testability and by using standard memories. TeakLite has a configurable memory size, a data-address-arithmetic unit, a multiplier, an ALU, four 36-bit accumulators, a bit-manipulation unit, and zero-overhead loop mechanisms for repeat and block repeat. Its instruction set includes microcontroller instructions enabling high code density. It has user-definable registers for hardware acceleration, coprocessor support, or both; cycle-stealing DMA support; and active, slow, and ideal power-management-operation modes.

The VoPStream, previously known as VoPKey, is a licensable design for VoP (voice-over-packet) applications. The company based VoPStream on the TeakLite DSP architecture. It targets VoDSL (voice-over-DSL), VoCable (voice-over-cable), enterprise/residual gateways, and IP-PBX (Internet protocol-private-branch exchange) and IP (LAN) phone applications. VoPStream can operate alone, or you can use it as a subsystem in an integrated-networking/VoP SOC. VoPStream includes software for speech compression and decompression, echo cancellation, and other associated telephony functions. The software is open, allowing designers to add proprietary algorithms. An evaluation board is available, based on a mass-production chip that incorporates the VoPStream design and includes a set of development tools. The DSP firmware includes speech codecs, such as G.723, G.726, G.729 and G.711, G.168 echo cancellation, VAD, CNG, DTMF fax/modem detection, caller ID, and many more algorithms.

Addressing and processing modes: TeakLite supports register, single- and double indirect, short- and long-immediate, short- and long-index, stack-pointer, and program-memory-indirect addressing modes. It supports circular (modulo) buffering for all its pointers and direct addressing for the entire 64k-word

data space. VoPStream supports synchronous and asynchronous interfaces to external memories, such as DRAM and flash for data storage. VoPStream can function as a slave device using the host-port interface. It can communicate with pulse-code-modulation devices and E1/T1 standard peripherals using SPI and time-division-multiplexing interfaces.

Special instructions or integral-peripheral functions: Instructions include single-cycle minimum/maximum calculation with pointer latching, double-precision calculations, normalization, single-cycle exponent evaluation, conditional accumulator modifications, division step, read-modify (add/subtract/OR/AND/XOR)-write, test 16-bit mask bits and test bit, delayed return, interruptible single-word repeat loop and block repeat, 36-bit shift left or right in a single cycle, and a bank exchange of alternative registers. It also has support for program boot and code downloading. The VoPStream on-chip serial port permits direct interface with PCM highways or to ADCs and DACs, and the 8/16-bit host port permits interfacing to a variety of host processors, including PowerPC, ARM, and MIPS. The VoPStream includes four optional on-chip sigma-delta analog codecs.

Development support: ParthusCeva provides GUI-based development tools for all the DSP cores and platforms. These tools include an optimizing C++/C-compiler, an assembler, a linker, common-object-file-format converters, a debugger with an emulation interface and a Matlab interface, the Assyst extendable simulator for system-on-chip simulation, a profiler, and the ability for multicore debugging. ParthusCeva offers evaluation-development boards for each core for specific market segments, such as image, video and VoIP (voice-over-IP), and for integrating with RISC architectures. ParthusCeva offers various algorithms, such as speech codecs, audio, and video, as well as technical training courses and design services. ParthusCeva's infrastructure of third-party vendors offers software algorithms, development tools, and design services.

PHILIPS SAF7730

at a glance:

- Fully integrated audio and radio processing includes ADCs and DACs.
- The device integrates two independent radio-reception paths.

The SAF7730 mixed-signal DSP targets the automotive-car-radio market. The multicore DSP integrates several Philips DSP cores for audio and radio processing, and it integrates analog IF input, digital-radio and audio processing, sample-rate converters, and digital and analog audio output into a single device. The DSP core features a double Harvard architecture and uses a fixed-point, 2's complement notation for 24 bits of data and 12 bits of coefficients. It combines a high clock frequency and double-precision arithmetic, allowing designers to obtain high total-harmonic-distortion and SNR performance.

Addressing and processing modes: The SAF7730 supports direct and relative addressing. Relative addressing supports decrementing the pointer by one or incrementing it by one or two.

Special instructions or integral-peripheral functions: The SAF7730 includes a delay line unit, a data I/O unit, a multiplier-accumulator unit, and a microprocessor interface for μP control.

Development support: Philips offers an assembler, a simulator, an application board, and a real-time

GUI-based monitor program. Philips has defined assembler-code-flow and application templates to enable integration of library modules from the audio-feature library, which includes a set of efficient filter implementations, into target applications.

RC MODULE NEUROMATRIX NM6403

at a glance:

- The vector coprocessor can handle variable-length, 1- to 64-bit data.
- Variable-length data enables speed and precision trade-offs.

RC Module's NeuroMatrix NM6403 dual-core, application-specific DSP is based on the NeuroMatrix architecture targeting video-image processing and neural-network applications. It provides scalable performance, a programmable operand width of 1 to 64 bits, and operation as fast as 50 MHz. This flexibility allows designers to trade precision for performance to suit their applications. The NM6403 processor includes a 32/64-bit RISC processor and a 1- to 64-bit vector coprocessor that supports vector operations with elements of variable bit lengths (patent pending). Two identical programmable interfaces work with external memory, and two communication ports are hardware-compatible with Texas Instruments' TMS320C4x, allowing designers to build multiprocessor systems.

The vector coprocessor, which has an SIMD (single-instruction-multiple-data) architecture, works on packed integer-data comprising 64-bit blocks in the form of variable 1- to 64-bit words. The device supports vector-matrix or matrix-matrix multiplication. The Vector coprocessor's core looks like an array multiplier comprising cells that include a 1-bit memory (flip-flop) surrounded by several logical elements. Designers can combine the cells into several macrocells with two 64-bit programmable registers. These registers define the borders between rows and columns with macrocells. Each macrocell performs the multiplication on variable-input words using preloaded coefficients and accumulates the result from the macrocells in the column above it. The columns simultaneously calculate the results in one processor cycle. For 8-bit data and coefficients, the vector coprocessor performs 24 MAC (multiply-accumulate) operations with 21-bit results in one 20-nsec processor cycle. The number of MAC operations depends on the length and number of words packaged into a 64-bit block. The engine's configuration can change dynamically during calculations. An application can start with maximum precision and minimum performance and dynamically increase performance by reducing the data-word lengths. To avoid arithmetic overflow, the NM6403 uses two types of saturation functions with user-programmable saturation boundaries.

The VLIW (very-long-instruction-word) RISC core uses a five-stage pipeline that operates with 32- and 64-bit-wide instructions. Each instruction usually executes two operations. Two 64-bit interfaces support SRAM, DRAM, and EDO DRAM and comprise two separate address-generation units that can address as much as 16 Gbytes. Each interface supports two memory banks and can support a "shared-memory" mode. Two DMA coprocessors transfer data between high-speed I/O-communication ports and external memory.

Addressing and processing modes: The NM6403 supports 32-bit immediate, base, indexed, and relative addressing.

Special instructions or integral-peripheral functions:The NM6403 processor uses vector instructions to handle packets of as many as 32 64-bit data words. These instructions may define operations such as matrix-matrix, matrix-vector, or vector-vector multiplication; vector-vector addition and subtraction with saturation of results; block moving; and bit manipulation. The NM6403 has conditional branch, call, and return instructions.

Development support: The NeuroMatrix Software Development Kit for PCs includes an ANSI X3J16/95-0029 preliminary-standard-compatible C++ compiler, an assembler, an instruction-level simulator, a cycle-accurate simulator, a linker, a source-level debugger, a load/exchange library, and a set of application-specific vector-matrix libraries. RC Module offers PCI and CompactPCI evaluation/development boards for real-time DSP and video-image-processing designs. The vector-matrix library simplifies C-language programming for FFT, DCT, Sobel, and Hadamard Transform. RC Module also provides a NM6403 Verilog behavioral model for Sun host platforms for system-level simulation and a synthesizable core targeting Samsung and Fujitsu semiconductor technologies.

SENSORY RSC-XX

at a glance:

- RSC processors are specialized for speech recognition and synthesis.
- RSC processors support noise-robust speech recognition and high-quality, 5-kbps speech output.

The RSC-3x and RSC-4x speech processors combine a microcontroller with advanced speech-processing technology targeting high-quality speech recognition, speech and music synthesis, speaker verification, and record and playback. These devices feature a high-performance microcontroller with generous on-chip RAM and ROM, and DSP blocks, such as an independent digital filter bank and a multiplier. The RSC-4x family also features a vector processor to accelerate signal processing.

The RSC-3x and RSC-4x use a neural network to perform speaker-independent speech recognition. Both achieve high-quality speech-synthesis output using time- and frequency-domain-compression techniques. The RSC-4x uses Sensory's SX compression technology supporting speech playback data rates as low as 5 kbps. The RSC-4x features Hidden Markov Model speech recognition enabling text-to-speaker-independent generation of noise-robust recognition sets with just a few keystrokes. Designers have access to 24 I/O lines for general-purpose product control.

Addressing and processing modes: RSC devices support sequential addressing modes. Sensory has expanded the RSC-4x address space to 1 Mbyte.

Special instructions or integral-peripheral functions:The RSC-3x and RSC-4x processors include an on-chip microphone preamplifier and ADC for speech input and a DAC with optional amplification for speech output. This configuration enables a single-chip option for speech-in/speech-out dialogue applications. Enabling true continuous listening in battery applications, the RSC-4x includes an audio-wake-up feature that monitors the environment independently of the microcontroller, and an audio event triggers the chip to wake from a 50-mA sleep mode. Sensory has added new 16-bit data instructions to the RSC-4x. The RSC-4x family features twin DMA units, as many as four comparator

inputs, a watchdog timer, and as many as eight nested interrupt sources for power-saving wakeup.

SENSORY SC-6X

at a glance:

- SC-6X supports speech synthesis in bit rates covering a range of quality and memory requirements.
- As many as 14 channels of music or 10 channels of music simultaneous with speech are possible

The SC-6x DSP family targets speech- and music-synthesis applications. The Sensory speech algorithms support long-duration speech with data rates as low as 1 kbps using MX and the industry's highest quality using CX. Six fixed-bit rates of CX, beginning at 3 kbps, and a variable range of MX bit rates are available to mix and match your quality and memory requirements. The SC-6x family supports 14-channel, polyphonic music and as many as 10 channels of music simultaneously with speech playback. These DSPs support three low-power modes, two timer interrupts, one DAC interrupt, and five general-purpose interrupts to improve battery life and response speed to button and keyboard presses. The SC-6x devices include 32 I/O lines to support speech and music synthesis and general-purpose product control with interactive interfaces.

Addressing and processing modes: The addressing modes are immediate, direct, indirect-with-postmodification, and three relative modes. The program-counter unit comprises the program counter, the data pointer, a buffer register, a code-protection write-only register, and a hardware-loop counter for strings and repeated-instruction loops. It provides addressing for program memory (onboard ROM) and includes a 16-bit arithmetic block for incrementing and loading addresses. The program-counter unit generates a ROM address as output.

Special instructions or integral-peripheral functions: The SC-6x processors offer instructions to facilitate filtering algorithms, such as FIR, FIRK, COR, and CORK. FIR is useful for adaptive filtering or applications in which coefficients come from an external source. COR instructions perform 16×16-bit multiplies and 48-bit accumulation in three clock cycles. Instructions are available to perform 16×16-bit multiplies and 32-bit accumulation in two clock cycles.

Development support: The RSC and SC-6x development-tool suite includes an in-circuit emulator with an integrated debugger and a C compiler. Quick T2SI allows text entry and generation of recognition sets, and Quick Synthesis and the SCT6000 tool provide “pushbutton” speech compression. A tool for integration of MIDI-format music in an SC-6x application includes a rich selection of music voices (instruments). Demonstration units and evaluation and prototyping tools, such as the Voice Extreme Toolkit, are available. Each kit includes required hardware and software, complete documentation, and numerous examples. Turnkey product-development and linguistics services are available directly through Sensory or through its worldwide network of third-party-development houses.

SIROYAN SRXXX and ONEDSP ARCHITECTURE

at a glance:

- The VLIW DSP architecture can scale to as many as 32 dual-issue clusters.
- OneDSP can perform as many as 25.6 billion MACs at 200 MHz.

Siroyan's OneDSP architecture uses VLIW (very-long-instruction-word) and clustering techniques to provide scalable, high-performance DSP power allowing as many as 32 execution-unit clusters in a single core. Prevalidated configuration options include setting the number of clusters and endianness, as well as the cache-memory size and configuration. Each cluster consists of general-purpose registers, accumulators, a number of execution units, cache memory, local memory, and an on-chip bus interface. The master cluster executes either scalar RISC instructions from its instruction cache or VLIW instructions from its V-cache. In multicluster designs, VLIW instructions issue in parallel from the V-cache in each of the slave execution-unit clusters.

The foundry-independent SRA328 is the first implementation of the OneDSP architecture and enables SOC (system-on-chip) designers to deploy one to eight execution-unit clusters with 32-bit datapaths in single IP (intellectual-property) core. The core targets a range of applications, from wireless communications to digital control and speech processing. The SRA328 offers a choice of architectural configurations, memory subsystems, and selectable, application-specific instructions. A combination of architecture-design and process optimizations, including shutting down clusters when they're not in use and a variety of power-down modes, contribute to the system's power efficiency.

Addressing and processing modes: In addition to normal RISC addressing modes, OneDSP supports autoincrement, autodecrement, circular-buffer, and bit-reversed addressing modes.

Special instructions or integral-peripheral functions OneDSP supports Galois-field arithmetic for Reed-Solomon-coding applications and encryption algorithms. The SRXXX cores have an integrated DMA engine capable of basic scatter/gather functions and bit-reversed addressing and ships with a sample system that includes an AMBA AHB and an APB bus system, an external memory interface, and an area of on-chip SRAM.

Development support: Siroyan's OneDSP development environment runs on Unix, Linux, or Windows OSs. The debugging interface connects via a Nexus 5001 interface to a debugging adapter, offering Class 4-compliance at rates reaching 100 MHz. A debugging adapter is available for connecting the debugging board on the target development board to the host computer via Ethernet, allowing programmers to share target boards. Siroyan supplies a tool chain for application-software development, including a Gnu C compiler for scalar code, an optimizing C compiler for both scalar and VLIW code, an assembler, a debugger, and an OS kernel. Siroyan also works with third-party developers to deliver software and tools.

STARCORE STARCORE DSP

at a glance:

- StarCore supports user-defined instructions.

StarCore is a new company established to license IP (intellectual property) of the StarCore DSP and peripheral blocks. This synthesizable DSP core uses a fixed-point architecture with an extensible, 16-bit

instruction word, and it targets communications applications, such as 2.5, 2.75, and 3G mobile handsets, wireless base stations, and communication-infrastructure devices. Low power dissipation helps extend battery life and meet power-per-channel budgets. The StarCore DSP employs parallelism to enable compact code that requires smaller memories. Designers can use a single DSP architecture and reuse key kernels and code for midlevel as well as advanced applications.

Addressing and processing modes: The StarCore DSP architecture supports register-direct mode, address-register-indirect mode, and program-counter-relative modes. For address-register-indirect modes, the architecture supports linear, reverse-carry, modulo, and multiple-wraparound-module arithmetic types.

Special instructions or integral-peripheral functions: The StarCore DSP multipliers support all combinations of signed and unsigned operands and both fractional and integer formats. The architecture supports an SIMD (single-instruction-multiple-data) version of maximum and minimum additions and subtractions (MAX2, ADD2, SUB2). It can perform eight 16-bit additions or maximum and minimum operations per cycle and includes MAX2VIT, which works with Viterbi shift left to accelerate Viterbi decoding algorithms. A user-defined instruction-set-accelerator module enhances the StarCore DSP standard instruction set.

Development support: StarCore provides direct support as well as services, including macro hardening, design support, and training for implementing a DSP core into an SOC (system on chip). It has established alliances with a network of leading third-party tool providers, OSs, and application software, giving developers alternatives to choose from, including Metrowerks (www.metrowerks.com), GreenHills (www.ghs.com), Altium/Tasking (www.tasking.com), Quadros (www.quadros.com), OSE Systems (www.ose.com), Trinity Convergence (www.trinityconvergence.com), Signals and Software (www.signalsandsoftware.com), HelloSoft (www.hellosoft.com), and Numerix (www.numerix-dsp.com).

STMICROELECTRONICS ST100

at a glance:

- The ST122 can perform 1.2 MMACs (million MACs)/sec at 600 MHz.
- Interfaces support customizable co-processors.

The general-purpose, 16-bit, fixed-point ST100 family architecture is suitable for integration into SOCs (systems on chip) targeting wired- and wireless-communications, automotive, or multimedia applications. The instruction set features DSP instructions as well as 32- and 16-bit microcontroller instructions for enhanced performance and code density. The architecture supports a 4-Gbyte memory space, 40-bit registers and accumulators, four idle modes for power-consumption reduction, and three zero-overhead nestable loops. It is scalable between high-performance and low-power operation.

Addressing and processing modes: The ST100 family supports 13 addressing modes-including circular, which suits FIR filtering, and bit reverse, which optimizes FFT implementations. Data-memory accesses handle bytes, half-words (16 bits), and words (32 bits).

Special instructions or integral-peripheral functions: The instruction set supports predication for most of its instructions, packed arithmetic, and a special instruction for Viterbi. The ST122 core supports dual 16×32-bit MAC (multiply-accumulate operations) for audio applications and multimedia-specific instructions. The ST122 subsystem includes a scalable program-cache-memory interface, which dedicated program-cache instructions control. The ST122 core can interface with as many as four tightly coupled coprocessors to improve system performance and power consumption.

Development support: STMicroelectronics and third-party partners, such as Green Hills (www.ghs.com) and OSE Systems (www.ose.com), offer a complete suite of evaluation boards, software-development tools, and application-software libraries to support hardware and software developments of ST100-based SOCs. Development tools are available for Windows and Unix host systems.

TENSILICA XTENSA CORE WITH VECTRA DSP ENGINE

at a glance:

- Extensible core offers additional user-defined execution units and instructions.
- DSP options include dual or quad multiply-accumulate unit.

Tensilica's Xtensa V processor is a configurable, extensible, and synthesizable processor core. Designers can add DSP extensions via a Web-based configurator as well as application-specific instructions to define new registers, register files, and custom data types. The Xtensa processor generator automatically builds a correct-by-construction RTL description as well as a software tool set that incorporates the new instructions. The base architecture includes a 32-bit RISC ALU, as many as 64 general-purpose registers, and 80 base instructions, including 16- and 24-bit RISC instruction encoding with combined branch instructions, such as combined compare-and-branch and zero-overhead loops, and bit manipulations, including funnel shifts and field-extract options.

DSP engines in the Vectra family are fixed-point coprocessors for Tensilica's Xtensa architecture. The Vectra DSP engines use an SIMD (single-instruction-multiple-data) architecture that allows vector registers to maintain data, coefficients, and intermediate results of an algorithm. The Vectra engine's large vector register file helps reduce memory-bandwidth requirements and improves overall system performance. The Vectra engine supports single- and double-width operand sizes for greater computational accuracy. The Vectra instruction set extends the capability of the basic Xtensa microprocessor core.

Addressing and processing modes: Xtensa supports both little-endian (PC-compatible) and big-endian (Internet-compatible) address models as a configuration parameter and provides optional support for zero-overhead loops and an MMU with multiple memory-protection modes. Xtensa supports 8-, 16-, 32-, 64-, and 128-bit memory references. The Vectra DSP engine's four addressing modes include immediate and indexed with or without updates to the base register.

Special instructions or integral-peripheral functions: Configuration options include multipliers and MACs, DSP engines, a floating-point unit, variable processor-interface width (32-, 64-, or 128-bit), big and little-endian byte ordering, on-chip debugging, a trace port, XLMI high-speed local interface, as

many as 32 interrupts, memory-management options, local data and instruction caches, and separate ROM and RAM areas. Compound instructions include special shifts, compare/branch, and zero-overhead loop instructions. Special Vectra instructions include vector operations for load/store, arithmetic (add, multiply), binary operations, and bit packing and unpacking.

Development support: Designers use the Xtensa Processor Generator to configure and extend a family of core processors with application-specific functions. The Xtensa Processor Generator also automatically generates a complete suite of development tools, including a compiler, an assembler, a linker, and a debugger that match the particular Xtensa/Vectra hardware implementation. Tensilica also provides a cycle-accurate instruction-set simulator, and a bus functional model.

Tensilica offers five main development tools, including a GNU-based software-development suite, the XCC (Xtensa C/C++ compiler), the instruction-set simulator and XTMP (Xtensa Modeling Protocol) API, the Mentor Graphics Xray debugger, and the TIE (Tensilica-instruction-extension) compiler. Third-party support includes Accelerated Technology's (www.acceleratedtechnology.com) Nucleus Plus RTOS with Xtensa OSKit for Nucleus Plus and codelab developer suite, Wind River's (www.windriver.com) VxWorks RTOS and the Tornado 2 development platform, Monta Vista's (www.mvista.com) Hard Hat Linux, Sophia Systems' (www.sophia.com) UniStac Xtensa (JTAG) in-circuit emulator, and Macraigor Systems' (www.macraigor.com) Wiggler on-chip-debugging tool. Available third-party peripheral intellectual property includes AC3 decoder, Bluetooth, G723-1 Codec, G729AB Codec, MPEG-2 AAC decoder, MPEG-4 AAC decoder, MP3 encoder, MP3 decoder, and WMA decoder.

TEXAS INSTRUMENTS OMAP5910

at a glance:

- OMAP5910 integrates DSP and RISC cores targeting multimedia-rich applications.
- OMAP5910 offers system-on-a-chip functions with a flexible user interface.

The OMAP5910 embedded processor integrates a TMS320C55x DSP core with a TI-enhanced ARM925 on a single chip. The C55x DSP core has 64-kbyte dual-access RAM, 96-kbyte single-access RAM, 32-kbyte ROM, and three video-hardware accelerators (DCT/iDCT, pixel interpolation, and motion compensation). The C55x core has a six-channel DMA controller for high-speed data movement without DSP intervention. The ARM925 core is a 32-bit, pipelined RISC processor that performs 32- or 16-bit instructions and processes 32-, 16-, or 8-bit data. The ARM core includes an integrated LCD controller plus a 192-kbyte internal frame buffer. The OMAP5910 provides system DMA, multiple mailboxes, and a microprocessor-interface port for interprocessor communication.

Addressing and processing modes: The C55x DSP core supports single-data-memory-operand addressing that 32-bit operands. It also supports dual-data-memory-operand addressing that parallel instructions use. The C55x DSP core supports absolute addressing, register-indirect-addressing, direct-addressing, and displacement mode. The C55x includes dedicated registers to support circular addressing for instructions that use indirect addressing.

Special instructions or integral-peripheral functions: The C55x DSP core has special instructions

that can combine instructions to perform two operations. You can combine built-in parallel instructions with user-defined parallel instructions. It can also perform dedicated-function instructions, such as FIR filters, single and block repeat, eight parallel instructions, and 10 multiply and eight dual-operand memory moves. The OMAP5910 includes an LCD controller, a camera interface, a USB 1.1 host and client, an MMC/SD (multimedia-card/secure-digital)-card interface, a keyboard, infrared support,² C, Microwire, eight timers, a real-time clock, a nine-channel system DMA, eight serial ports, three UARTs, and hardware-video accelerators.

TEXAS INSTRUMENTS TMS320C2000

at a glance:

- Devices combine performance and peripheral integration for the embedded-control industry.
- These code-compatible DSPs target embedded-control applications.

The TMS320C2000 family of 17 code-compatible DSP controllers offer a combination of on-chip peripherals, such as flash memory, fast ADCs, and CAN modules targeting embedded-control applications, such as consumer and industrial-control applications—including motor control, white goods, HVAC, power tools—automotive, power supply, and optical-networking. The TMS320C24x is a 16-bit DSP core. The TMS320F2810 and TMS320F2812 DSPs are 32-bit control DSPs with onboard flash memory and performance to 150 MIPS. The C28x core offers 300 MIPS of computational bandwidth with a signal-processing core optimized for control. It is fully code compatible with current devices in the C2000 family.

Addressing and processing modes: The C2000 DSP platform supports indirect and direct addressing.

Special instructions or integral-peripheral functions: The C2000 DSP platform integrates flash memory, a 12-bit ADC, an event manager optimized for pulse-width-modulation generation, CAN modules, and serial interfaces. The C28x also features a C-to-assembly ratio of 1-to-1 that allows developers to write their algorithms in a high-level language. These devices support “virtual-floating-point” programming that provides a floating-point machine on a fixed-point architecture.

TEXAS INSTRUMENTS TMS320C5000

at a glance:

- The C5000 DSP platform offers more than 30 code-compatible devices.
- C5501 and C5502 are 300-MHz, dual-multiply-accumulate-unit DSPs with less than 200 mW power dissipation that cost less than \$10.

The TMS320C5000 DSP platform has more than 30 code-compatible devices and includes the TMS320C54x and TMS320C55x DSP generations. These devices use a modified Harvard architecture and target portable Internet, multimedia communications, and medical and biometrics applications. The TMS320C5420 and TMS320C5421 are both dual-core devices, and the TMS320C5441 is a quad-core

device targeting high-channel-density applications. The TNET3010 has six C55x DSP cores, targeting high-density voice and access class E1/T1 telecom applications. Compared with a Pentium 4, it has three times the transistor count (approximately 180 million transistors), consumes 50 times less power, 20% smaller, and supports more than 200 voice channels.

The C55x DSPs are source-code-compatible with the C54x DSPs. The C54x focuses on low power consumption, but the C55x takes power efficiency to a new level: A 300-MHz C55x delivers a maximum fivefold improvement in performance over a 120-MHz C54x and dissipates as little as one-sixth its core power. The C55x has 12 independent buses, and the C54x has eight. Both architectures include one program bus and an associated program-address bus. The C55x bus is 32 bits wide, and the C54x bus is 16 bits wide. The C55x has three data-read buses and two data-write buses; the C54x has two data-read buses and one data-write bus. Each data bus also has its own address bus. The corresponding address buses are 24 bits wide on the C55x and 16 bits wide on the C54x.

Addressing and processing modes: The C54x supports single-data-memory-operand addressing that also supports 32-bit operands. It also supports dual-data-memory-operand addressing that parallel instructions use. It provides immediate, memory-mapped, circular, and bit-reversed addressing. In addition to the C54x modes, the C55x supports absolute addressing, register-indirect-addressing, direct-addressing, and displacement mode. The C55x includes dedicated registers to support circular addressing for instructions that use indirect addressing. Programs can simultaneously use as many as five independent circular-buffer locations with as many as three independent buffer lengths. These circular buffers have no address-alignment constraints. The C54x supports two circular buffers of arbitrary lengths and locations.

Special instructions or integral-peripheral functions: The C54x performs dedicated-function instructions, such as FIR filters, single and block repeat, eight parallel instructions, multiply, accumulate and subtract (10 multiply instructions), and eight dual-operand memory moves. The C55x also has special instructions that take advantage of the additional functional units and increase parallelism capabilities. User-defined parallelism allows you to combine instructions to perform two operations. You can also combine a built-in parallel instruction with a user-defined parallel instruction. The C5509 includes peripherals like a USB interface and multimedia-memory-card port.

TEXAS INSTRUMENTS TMS320C6000, TMS320DM642, AND TMS320DRI200

at a glance:

- Performance can scale from 1200 to 4800 MIPS.
- The TMS320DM642 consumes less than 1.5W of power.

The TMS320C6000 DSP platform, a general-purpose, VLIW (very-long-instruction-word) DSP architecture, targets advanced imaging, broadband, and wireless infrastructure. This architecture includes the fixed-point C62x and C64x DSP generations and the floating-point C67x DSP generation. The C6414, C6415, and C6416 DSPs offer maximum processor speeds of 600 MHz. These processors include large on-chip memories and target video and imaging, communications, and instrumentation applications. The C6411 device targets security, communications, and office-equipment applications. It is currently the lowest priced device in the C64x lineup, and it offers the lowest power of any device in the C6000 DSP platform. The C6713 is a floating-point DSP that is an upward migration path from the

C6711. It adds I²S, I²C, and S/PDIF transmit support as well as an enhanced memory space.

The TMS320DM642 is a fully programmable, 600-MHz digital media processor using a C64x core that includes integrated multimedia and communication peripherals targeting video over IP, video-on-demand, multichannel digital-video-recording applications, and video encoding and decoding. Its C64x DSP core processor has 64 general-purpose registers of 32-bit word length and eight independent functional units that include two multipliers for a 32-bit result and six ALUs with VelociTI.2 extensions. It can complete four 32-bit MAC (multiply-accumulate) operations per cycle.

The DRI200 handles the baseband processing for HD Radio and incorporates digital channel source, data decoding, and demodulation functions. The IDM combines the memory and appropriate interfaces on a credit-card-sized board. TI bases the DRI200 on the C64x core. It is compatible with iBiquity's (www.ibiquity.com) IBOC digital AM/FM system and can interface to an external microcontroller, DRAM, and SRAM. It is compatible with standard audio-DAC interfaces, includes JTAG emulation, and supports -40 to +85°C operation.

Addressing and processing modes: The C6000 DSP platform performs linear and circular addressing. Unlike other DSPs that have dedicated address-generation units, C6000 DSPs calculate addresses using one or more of its functional units. The DM642 performs dual 64-bit memory accesses each cycle and supports nonaligned memory accesses to enable sliding-window operations with SIMD (single-instruction-multiple-data) processing and circular addressing. The DM642 datapaths include support for packed data processing (SIMD), including quad 8-bit operations and dual 16-bit operations, useful for supporting video and image processing. Special instructions for key video-compression algorithms include sum-of-absolute differences for motion estimation and average instructions for motion compensation.

Special instructions or integral-peripheral functions: All C6000 DSP processors can conditionally execute all instructions, a method of reducing branching and thereby optimizing performance. On the C64x DSP, the MPYU4 instruction performs four 8×8-bit unsigned multiplies. The ADD4 instruction performs four 8-bit additions. Six of the C64x functional units can perform dual 16-bit addition/subtraction. Two of the functional units perform dual 16-bit compare, shift, minimum/maximum, and absolute-value operations. The M units also support dual 16-bit and quad 8-bit averaging operations as well as bit-expansion and bit-interleaving and -deinterleaving operations. Four of the six remaining functional units support quad 8-bit addition/subtraction operations. Two functional units support quad 8-bit compare and minimum/maximum instructions. Some instructions operate directly on packed 8- and 16-bit data. The C6411 peripheral set includes, two multichannel buffered serial ports; 32-bit, 33-MHz PCI; three timers; 64-channel enhanced DMA; and 32-bit external-memory interface. The C6414, C6415, C6416 peripheral set adds another multichannel buffered serial port, PHY interface for ATM (Utopia), and Viterbi and Turbo coprocessors.

The DM642 uses a two-level cache-based architecture. The Level 1 program cache is a 128-kbit, direct-mapped cache, and the Level 1 data cache is a 128-kbit, two-way set-associative cache. The peripheral set includes three configurable video ports; a 10/100-Mbps Ethernet media-access controller; a management data-I/O module; a VIC (VCXO interpolated control port); one multichannel buffered audio serial port; I2C bus module; two multichannel buffered serial ports; three 32-bit, general-purpose timers; a user-configurable 16- or 32-bit host-port interface; PCI; 16 general-purpose I/O pins; and a 64-bit, glueless external-memory interface that can interface to synchronous and asynchronous memories and peripherals.

TEXAS INSTRUMENTS TMS320DM310

at a glance:

- The processor consumes less than 500 mW.
- The processor provides real-time MPEG-4 video encoding and decoding.

The TMS320DM310 DSP-based programmable digital media processor integrates a C54x DSP core with an ARM9 32-bit RISC-processor core. It is one of the first devices of the digital-media-processor family to support real-time MPEG-4 video encoding and decoding at CIF (352×28-pixel) resolution and offers an integrated USB host supporting a direct-print capability. It is code-compatible with TMS320DSCx devices, and it supports both CMOS and CCD image sensors of as much as 6 million pixels with a less-than-1-sec shot-to-shot delay. Operating-system support includes Nucleus, Linux, Ultron, VxWorks, and WinCE.

Addressing and processing modes: The DM310 processor has an integrated SDRAM controller that supports SDRAM timing as fast as 100 MHz and provides continuous data access with low overhead.

Special instructions or integral-peripheral functions: The DM310 includes integrated USB-host and -device support, a real-time preview engine, integrated SRAM and external memory-interface controllers, 32 general-purpose I/Os, two serial ports, two multichannel, buffered serial ports, two UARTs, four timers, a watchdog timer, and seamless support for Compact flash, Smart Media, MMC/SD (multimedia-card/secure-digital) interfaces, and Memory Stick.

TEXAS INSTRUMENTS TMS320DSCX

at a glance:

- Device clock speed is 100 MHz.
- Device consumes less than 1W of power.

The TMS320DSC21, TMS320DSC24, and TMS320DSC25 DSPs digital-imaging systems on a single chip combine a TMS320C5000 DSP and an ARM7TDMI RISC processor targeting media-processing and system-control functions. The chips integrate a video encoder with an on-screen display, an SDRAM controller with a bandwidth-transfer rate of 320 Mbytes/sec, and a preview engine that performs 30-frame/sec NTSC and PAL previewing (DSC21/DSC25). The DSCx family of products can achieve real-time processing of a full-resolution 2 million-pixel image with a 1-sec shot-to-shot delay. DSCx DSPs can support the capture of high-resolution still photos and can record video clips with audio and music from the Internet. These systems support digital-audio and -video formats, including real-time MPEG-1, MPEG-4, JPEG, M-JPEG, H.263, and MP3, as well as data-communication standards, such as IrDA (DSC21), USB, and RS-232.

Addressing and processing modes: Addressing modes include SDRAM, SRAM, flash-media, and removable-media interfaces. The SDRAM transfer rate is 80 Mbytes/sec with both 332 (DSC21/24/25)

and 316 (DSC24) interface capabilities. The DSC24 enables 2-D-to-2-D data transfer from SDRAM to an on-chip image buffer, as well as direct SDRAM access via an SDRAM controller. The ARM can access the DSP via the host-port interface, and its bus controller has on- or off-chip access to general-purpose I/O, flash, Compact flash, and Smart Media applications.

Special instructions or integral-peripheral functionsIn addition to the TMS320C54x DSP-generation instruction set, the DSCx DSP subsystem incorporates imaging enhancements to provide fast-block-based processing for imaging or video-encoding and -decoding functions.

Development support: Texas Instruments' eXpressDSP real-time-software and development tools encompass development for all TMS320 devices and include the Code Composer Studio integrated development environment; the DSP/BIOS scalable real-time kernel, the TMS320 DSP algorithm standard set of coding conventions and APIs, and a third-party network. Evaluation modules, technical training classes, and customer-application support are also available.

The Innovator development kit for OMAP is a handheld, expandable, flexible development platform for OMAP. Code Composer Studio IDE for OMAP integrates all host and target tools into one environment, simplifying DSP configuration and optimization to take full advantage of the high-performance processing capabilities of the DSP core in the OMAP5910 device. CCStudio for OMAP addresses each phase of the code-development cycle, including designing, coding and building, debugging, analyzing, and optimizing. OMAP simulation includes both TMS320C5000 and ARM925 simulators for heterogeneous debugging.

The network-video-developer's kit for the C6000TM platform, based on ATEME's (www.ateme.com) IEKC64x, is an evaluation and development board using the TMS320C6416 DSP. This kit includes applications for image, video-stream, and audio compression. Software support for the DM310 includes modules for audio, video, and imaging compression and transmission standards, including MPEG-1, MPEG-2, MPEG-4, H.263, JPEG, M-JPEG, AAC, MP3, and Windows Media Audio. Additional support for software integration includes a DSP and ARM framework, providing a "plug-and-play"-like environment and evaluation modules. DM310's object code compatibility with DSC2x platform enable developers to begin programming using DSC platforms then port the development software to newer devices in the family as they become available.

3DSP SP-3, SP-5, AND SP-20/UNIPHY

at a glance:

- Cores enable single-chip multifunction digital imaging.
- 3DSP supplemented the SP-20/UniPHY core with additional IP to build 802.11a, b, and g subsystems.

The soft-IP (intellectual-property)-core, fixed-point DSP family, bus controller, peripherals, and microprocessor interfaces from 3DSP use a scalable 32-bit SuperSIMD (single-instruction-multiple-data) architecture. The core supports multiprocessor systems, program cache or direct-mapped program memory, 32 prioritized interrupts, 32 general-purpose I/O pins, and a JTAG-only debugging interface. The SP-3 core is a programmable, five-stage-pipelined DSP that targets MP3-player, home-audio (AAC, AC3), wireless-GSM-phone, GPS, and CPE

(customer-premises-equipment) VOP (voice-over-packet)-processing applications.

The SP-5 core is a programmable, superscalar, dual-issue, five-stage-pipelined DSP that targets 3G wireless, VOP gateway, xDSL, MPEG-2, MPEG-4, and wireless-LAN applications. The SP-5flex core is a fully synthesizable and configurable DSP core, based on the SP-5 architecture, which supports balancing power, cost, and performance. Designers can change the memory size, register-file size, and number of function units, and they can add application-specific instruction sets. The SP-5flex targets VOP, digital-wireless, audio, video, imaging, and broadband-modem applications. The SP-5V is a programmable, superscalar, dual-issue, five-stage-pipelined DSP that targets VOP applications.

The programmable, dual-mode, nine-stage-pipelined SP-20/UniPHY DSP IP core targets multimedia applications including multimedia over wireless. UniPhy can execute speeds of 400 MHz to 1 GHz because it supports a multiple-standard PHY implementation on the same processor. The “soft-datapath” technology and programmability enables a “softPHY” implementation that facilitates modification for changing physical-layer standards.

Special instructions or integral-peripheral functions:The 3DSP core supports two SIMD multiplier options. The first option is a dual 24×16 -bit multiply that can perform two 24×16 -bit multiplies, four 16×16 multiplies, or eight 8×16 multiplies in a single cycle. The second option is a dual 32×32 -bit multiplier that can perform all the functions of the 24×16 -bit multiplier and perform two 32×32 -bit multiplies in one cycle. The 32×32 -bit multiplier provides the highest quality audio processing.

The SP-20/UniPHY core combines accelerated versions of 3DSP’s SuperSIMD architecture and SP-x instruction set with an expansion-instruction mode that contains custom instructions targeting universal physical-layer signal processing for 802.11a/b/g, HiLAN2, and xDSL. Over the last year, 3DSP supplemented its SP-20/UniPHY core with additional IP to build an 802.11a, b, and g subsystem that includes a Viterbi accelerator, MAC (multiply-accumulate) accelerator, and radio interface that a suite of optimized software for the baseband and MAC (media-access controller) supports.

Development support: Offerings from 3DSP include SOC (system-on-chip) integration tools and services, including the DSP-Shuttle system-bus controller and the HiFI SOC-development environment as well as design services, for SOC integration. Developers using the DSP-Shuttle and HiFI software can progress from concept to silicon tape-out within nine months. The company also offers optimized suites of application software for multichannel-audio and MPEG4-video streaming multimedia, VOP, and wireless-LAN support.

The DSP-Shuttle is a high-speed, fully synthesizable and configurable DSP system-bus controller, based on the proprietary Intelligent DMA technology, to address the intense data flow of DSP applications. It features real-time and high-speed data transfer, dynamic data-dependent bandwidth allocation, and multicore support. It also provides a plug-and-play uniform interface to all system peripherals and enables low-power implementation.

The GUI-based HiFI SOC integration tool enables designers to co-develop hardware and software, configure the DSP core and memory subsystem, add peripheral devices, and test performance. They can use it to perform trade-offs among clock speed, area, and power consumption. The SOC integration tool includes Software Studio—a collection of software-development tools to edit, compile, assemble, optimize, debug, and manage application code.

Sketchpad development kits allow designers to optimize and evaluate the architectures, prototype hardware, and develop application software. The kits come ready for USB plug-and-play use with a Windows-based PC. All kits include a Sketchpad FPGA development board, Software Studio, power supply, and USB cables. Designers can download candidate hardware architectures onto the development board and evaluate the performance of each configuration using software for the application.

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