

1879BA1T

MIL-STD-1553B Interface Terminal

Features

- Complete integrated interface between host processor and MIL-STD-1553B data bus via external transceivers
- BC, RT, MT, simultaneous RT/MT modes
- 4Kx16 internal RAM, externally expanded to 64Kx16
- Flexible processor/memory interface:
 - ü 8- or 16-bit buffered mode
 - ü 16-bit transparent mode
 - ü 16-bit DMA mode
 - ü supports “Zero Wait” mode
- 16/12 MHz programmable clock rate
- Advanced BC features:
 - ü automatic retries
 - ü programmable gap times
 - ü frame auto-repeat
 - ü programmable response time-out
- Advanced RT features:
 - ü programmable illegalization
 - ü choice of single message mode, double buffering mode, and circular buffering mode
 - ü interrupts on individual mode codes
 - ü flexible data buffering
- Advanced MT features:
 - ü word monitor mode
 - ü selective message monitor mode
 - ü simultaneous RT/message monitor mode
 - ü trigger options
- Single +3.3V power supply, 5V-tolerant inputs
- 14 x 14 mm 80-pin LQFP package

Description

1879BA1T interface terminal provides complete, flexible interface between host processor and MIL-STD-1553B redundant data bus via external transceivers, implementing Bus Controller (BC), Remote Terminal (RT), Monitor Terminal (MT) or simultaneous RT/MT modes.

1879BA1T integrate encoder/decoder, complete BC/RT/MT multi-protocol logic, interrupt logic, control logic, memory management and processor interface logic, and 4K words of internal buffered SRAM. 1879BA1T may use up to 64K words of external SRAM at DMA configuration. 1879BA1T may be interfaced both to 16-bit and 8-bit microprocessors at shared memory mode. 1879BA1T may be operated at either 16 or 12 MHz software programmable clock rate.

1879BA1T BC and RT protocols implements all MIL-STD-1553B message formats, providing flexible interface to CPU and many advanced features. 1879BA1T implement three MT modes: word monitor, selective message monitor, simultaneous RT/message monitor, with trigger options.

1879BA1T require only single +3.3V power supply, provide CMOS output levels and have 5V-tolerant inputs. 1879BA1T comply with both Harris-compatible and Smiths-compatible MIL-STD-1553B data bus transceivers. 1879BA1T packaged at 14 x 14 mm 80-pin plastic LQFP with 0.5 mm pitch and have maximum height 1.7 mm that is well suited for applications with stringent height requirements.

Designed by RC MODULE devices 1553 terminals with 1879BA1T and various models of data bus transceivers were fully tested to compliance with MIL-STD-1553B requirements at S.P.Korolev RSC ENERGIA test house.

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1. Descriptions

1879BA1T fully integrated interface terminal provides complete, flexible interface between a host processor and a MIL-STD-1553B redundant data bus using external transceivers, implementing Bus Controller (BC), Remote Terminal (RT), Monitor Terminal (MT) or simultaneous RT/MT modes.

1879BA1T integrate encoder/decoder, complete BC/RT/MT multi-protocol logic, interrupt logic, control logic, memory management and processor interface logic, and 4K words of internal buffered SRAM. 1879BA1T may use up to 64K words of external SRAM at DMA configuration.

1879BA1T may be interfaced both to 16-bit and 8-bit microprocessors at shared memory mode, such as 680X0, i960, 80186, 8088, 6809, 8051, ADSP-2101 and others.

1879BA1T may be operated at either 16 or 12 MHz software programmable clock rate.

1879BA1T provide programmable options for interrupt generation and handling. The interrupt output has three software programmable modes of operation: pulse, level output cleared under software control, or level output automatically cleared following a read of the Interrupt Status register.

1879BA1T BC protocol implements all MIL-STD-1553B message formats. Message format is programmable on message-by-message basis by means of bits in the BC Control word and the T/R bit of the Command word for the respective message. The BC Control word allows 1553 message format, bus channel, self-test, and Status word masking to be specified on an individual message basis. In addition, automatic retries and/or interrupt requests may be enabled or disabled for individual messages. The BC performs all error checking required by MIL-STD-1553B. This includes validation of response time, sync type and sync encoding, Manchester II encoding, parity, bit count, word count, Status word RT address field, and various RT-RT transfer errors. BC response timeout value is programmable with choices of 18, 22, 50, and 130 μ s. The longer response timeout values enable operation over long buses and/or use repeaters.

1879BA1T RT protocol design implements all the MIL-STD-1553B message formats and dual redundant mode codes. RT protocol performs comprehensive error checking, word and format validation, and checks for various RT-to-RT transfer errors. RT protocol features include options for full software control of RT Status and Built-in-Test (BIT) words. These words may be formulated in real time by the protocol logic. Other key features include set of interrupt conditions, internal programmable subaddress-based command illegalization, programmable by subaddress BUSY bit, and flexibility of RT memory management architecture – 1879BA1T implement three RT modes: single message, double buffer, circular buffer.

1879BA1T implement three MT modes: word monitor, selective message monitor, simultaneous RT/message monitor.

After initializing of word monitor mode 1879BA1T stores all Command, Status, and Data words received. For each word received from either bus channel, 1879BA1T store information relating to bus channel, sync type, word validity, and interword time gaps. Monitor Trigger word provides additional flexibility for the word monitor mode: 1879BA1T have programmable options to start or stop the word monitor, and/or to issue an interrupt request following receipt of the Trigger word from the bus.

Selective message monitor provides features to greatly reduce the software and processing burden of host. Selective message monitor implements selective monitoring of messages from dual 1553 bus, with the monitor filtering based on the RT address, T/R bit, and subaddress fields of received Command words. Selective message monitor mode greatly simplifies the host processor software by distinguishing between Command and Status words.

Functional Diagram

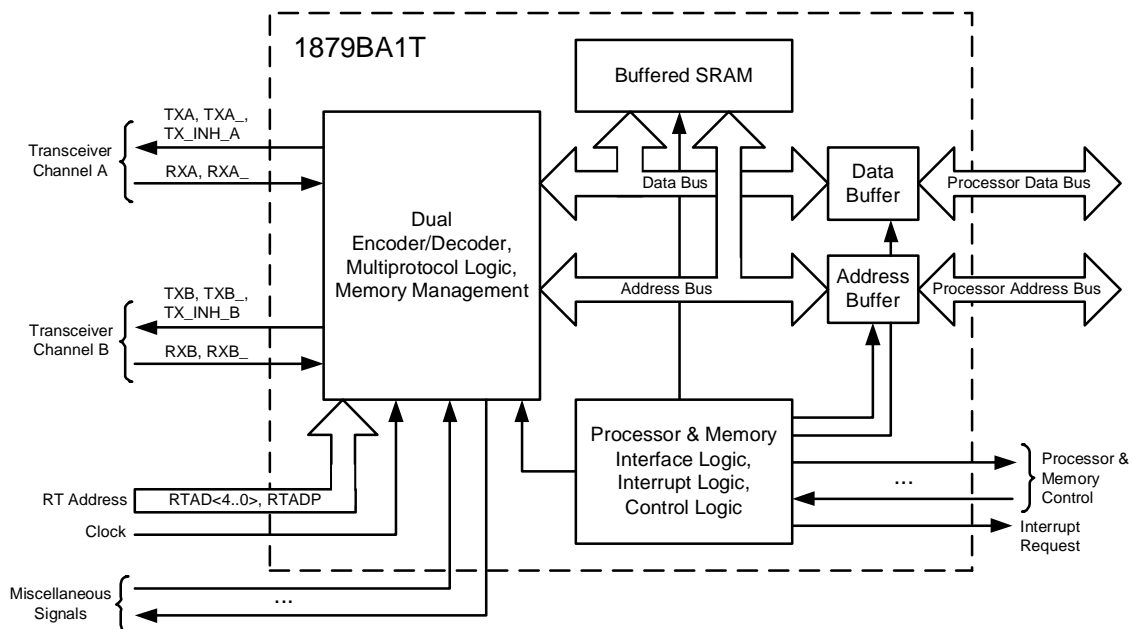
Selective message monitor may function as a purely passive monitor or may be programmed to function as simultaneous RT/message monitor. RT/message monitor mode provides complete RT operation for 1879BA1T strapped RT address and bus monitor capability for the other 30 non-broadcast RT addresses. This allows 1879BA1T to simultaneously operate as a full function RT and “snoop” on all or a subset of the bus activity involving the other RTs on bus. This type of operation is sometimes needed to implement a backup bus controller.

1879BA1T require only single +3.3V power supply, provide CMOS output levels and have 5V-tolerant inputs. 1879BA1T comply with both Harris-compatible and Smiths-compatible MIL-STD-1553B data bus transceivers.

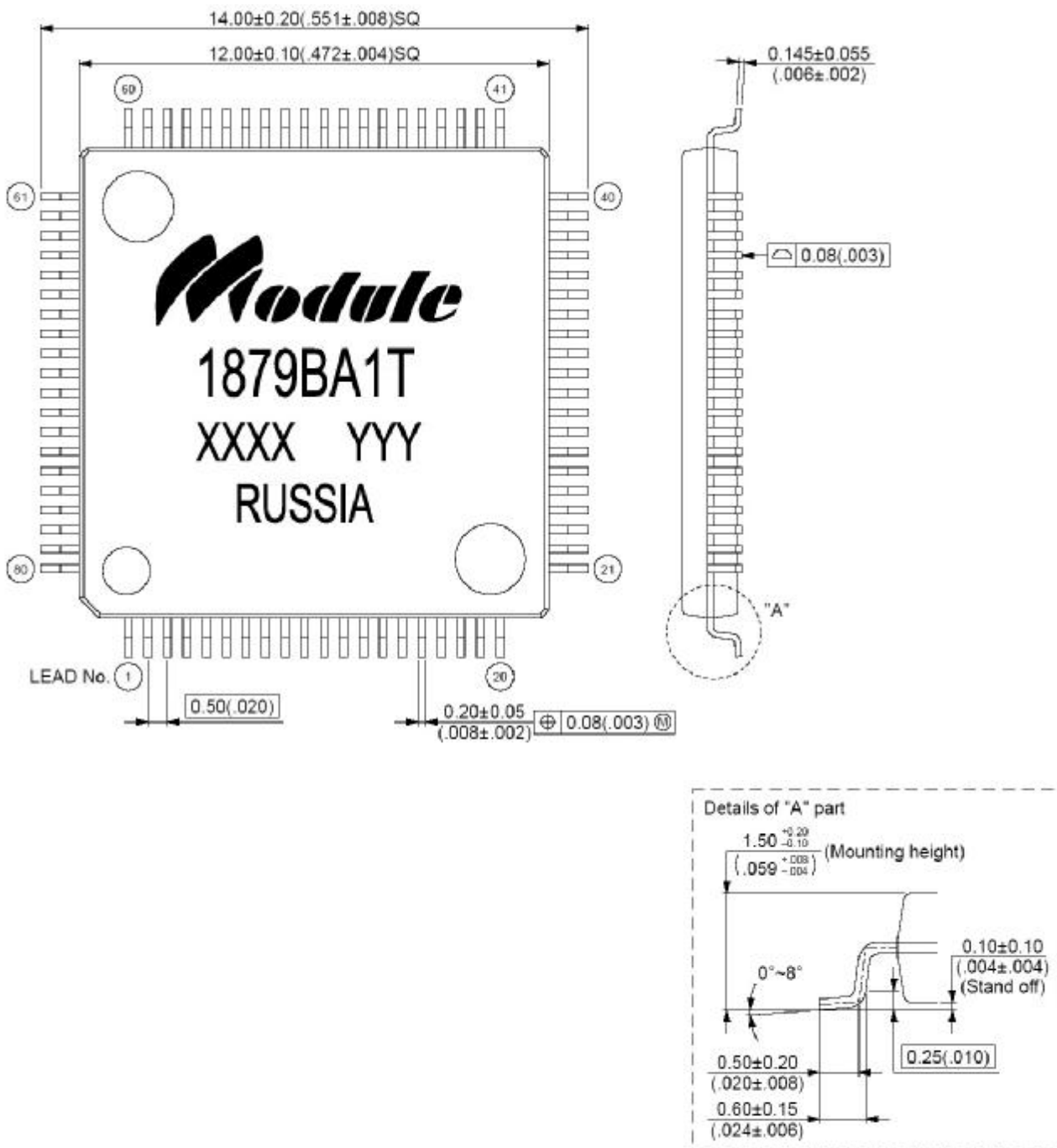
1879BA1T packaged at 14 x 14 mm 80-pin plastic LQFP with 0.5 mm pitch and have maximum height 1.7 mm that is well suited for applications with stringent height requirements.

Designed by RC MODULE prototypes of 1553 terminals with 1879BA1T and various models of data bus transceivers were fully tested to compliance with MIL-STD-1553B requirements at S.P.Korolev RSC ENERGIA test house.

2. Functional Diagram



3. Mechanical Outline



Notes:

- Dimensions in mm (inches)
- Pins width and pins thickness includes plating thickness
- XXXX: year/week code (example)
- YYY: control code (example)

4. Pin Listing

Pin	Signal Name	Pin	Signal Name
1	A13	41	INCMD*
2	VSS	42	VSS
3	A12	43	D00
4	A11	44	D01
5	A10	45	D02
6	A09	46	D03
7	A08	47	D04
8	A07	48	D05
9	A06	49	D06
10	A05	50	D07
11	MEMENA_OUT*	51	MEMOE*/ADDR_LAT
12	VSS	52	VSS
13	VDD	53	VDD
14	A04	54	D08
15	A03	55	D09
16	A02	56	D10
17	A01	57	D11
18	A00	58	D12
19	DTREQ*/16/8*	59	D13
20	DTACK*/POLARITY_SEL	60	D14
21	DTGRT*/MSB/LSB	61	D15
22	VDD	62	VDD
23	VSS	63	VSS
24	MSTCLR*	64	MEMWR*/ZERO_WAIT*
25	SSFLAG*/EXT_TRIG	65	RXA
26	TAG_CLK	66	RXA_
27	TRANSPARENT/BUFFERED*	67	TX_INH_A
28	STRBD*	68	TXA
29	SELECT*	69	TXA_
30	MEM/REG*	70	TXB
31	RD/WR*	71	TXB_
32	CLOCK_IN	72	TX_INH_B
33	VDD	73	VDD
34	MEMENA_IN*/TRIGGER_SEL	74	RXB
35	RTAD0	75	RXB_
36	RTAD1	76	INT*
37	RTAD2	77	READYD*
38	RTAD3	78	IOEN*
39	RTAD4	79	A15
40	RTADP	80	A14

5. Specification

Parameter	Min	Typ	Max	Units
Absolute Maximum Rating - Supply Voltage - Input Voltage - Output Current	- 0.4 - 0.5 - 13		4.0 6.0 13	V V mA
Power Supply - Supply Voltage (VDD) - Supply Current	3.0	3.3	3.6 200	V mA
Load Capacitance - Output & Bi-directional Load Capacitance			50	pF
Logic (VSS = 0V) - H-level Input Voltage - L-level Input Voltage - Input Leakage Current - H-level Output Voltage - L-level Output Voltage - Output Current	2.0 VSS - 10 VDD - 0.5 VSS - 4		5.5 0.8 10 VDD 0.4 4	V V µA V V mA
1553 Message Timing - Completion of CPU Write (BC Start to Start of Next Message) - BC Intermessage Gap (Software Programmable) - BC/RT/MT Response Timeout: - 18.5 Nominal - 22.5 Nominal - 50.5 Nominal - 128.0 Nominal - RT Response Time - Transmitter Watchdog Timeout		2.5 668		µs µs µs µs µs µs µs
Physical Characteristics - Size (maximum values) - Weight (maximum value)		14.2 x 14.2 x 1.7 0.47		mm g

6. Applications

Interfacing of host processors to MIL-STD-1553B redundant data bus at avionics and other mission-critical applications, development of hardware and software test systems.



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